

Test Challenges of Nanometer Technology

Janusz Rajski
Chief Scientist and Director of DFT Engineering
Mentor Graphics Corporation

DFT. The last 30 years have demonstrated that short time-to-market, low cost, and high product quality can only be achieved if test is part of the design and optimized for manufacturing. Structural DFT methodologies based on scan with voltage-based test, supplemented by Iddq test, provided predictable test quality and a basis for automation of test synthesis and test pattern generation. Scan also provided effective means for silicon debug and diagnostics. Memory BIST has been widely adopted for testing embedded memories.

Test quality. Nanometer technologies introduce new formidable challenges making test quality an even faster moving target. Complex copper interconnects, low-k dielectric materials, and new manufacturing processes completely change defect distributions. There are more node-to-node bridges undetected by tests for stuck-at faults, more node-to-node resistive bridges that require at-speed test, more in-line resistance caused by defective vias, and more cross-talk effects undetected by Iddq tests. Numerous small delay defects are detected only when they propagate to outputs with a small slack.

Cost of test. With fading effectiveness of Iddq test, unaffordable functional patterns, combined with cost and reliability related restrictions on burn-in test, the fundamental challenge is to provide adequate and cost-effective product quality through scan test. These factors rapidly increase the number of at-speed scan patterns. In addition, SOC design styles combined with nanometer technology allow for massive integration resulting in explosion of gate count and volume of test data. At the same time there is a need to reduce the cost of test by reducing test time, volume of test data, and limiting the required number of tester channels, tester frequency, and tester accuracy.

Embedded test. In order to meet the short time to market, low cost, and high product quality requirements, test solutions for nanometer technologies will predominantly depend on enhanced embedded structural DFT methodology with four important characteristics:

1. **Robust defect-alert patterns** with significantly improved ability to detect real defects and design marginalities will be essential to guarantee good product quality.
2. **Test compression** with a very large number of internal scan chains driven by on-chip decompressors and observed by on-chip compactors will be necessary to address the I/O bandwidth and reduce cost of test.
3. **At-speed capture** controlled by on-chip clocks will provide the means to deliver at-speed patterns required for high quality test while decreasing the dependence on tester frequency and accuracy, and reducing cost of test.
4. **Automated silicon debug and yield improvement** based on scan will be necessary to deal with the increased problem complexity and will be crucial in achieving short time-to-market requirements.

Invited Address



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Chief Scientist and
Director of DFT Engineering
Mentor Graphics Corporation

About the Speaker

Janusz Rajski holds a Ph.D. degree from the Poznan University of Technology, Poland. He is Chief Scientist and Director of DFT Engineering at Mentor Graphics Corporation. He has published over 100 technical papers on ATPG, Logic BIST, embedded forms of deterministic test, and logic synthesis. His factorization and decomposition algorithms have been adopted in many commercial and industrial synthesis tools. He holds 12 US patents in the area of test. He is also the principal inventor of Embedded Deterministic Test (EDT™) technology and architect of TestKompress™. Janusz received a number of awards including the ITC 1999 Honorable Mention award for work on Logic BIST.