

Panel: “Board test and ITC: what does the future hold?”

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The International Test Conference is becoming a chip-centric event. This is what you might expect to be told. And if you ask which conference a board test engineer should attend in order to get information about innovation in the field of board test, the answer may be: there are several exhibitions dealing with electronic manufacturing, there you can find what you are looking for. Unfortunately, the audience of this kind of expositions is not interested in innovation if the same innovation is not supported by a commercial solution available on the market. Therefore, a researcher is scarcely motivated in attending those exhibits and explaining his smartest solution for a single problem. If no researchers are attending the event, the event itself has not the same appeal. On the other side, the board test engineer might wonder why board test was not among the hot topics during last years at ITC, i.e. which is the scenario of innovation in the field of board test: does board test suffer from a lack of academic interest? Or, perhaps, are board test engineers used to talk with researchers about their needs?

Several techniques for prototype and production board test are very well known and applied, and perhaps they do not need further investigations. This is the case of the In Circuit Test through nails or flying probes, the Automatic Optical Inspection (AOI), some programmable devices configuration techniques, and so on. Moreover, other test techniques are well known (e.g. Boundary Scan, XRay Inspection, techniques based on the new standards IEEE 1149.4, 1149.6, 1532), but not yet very well supported by the tool/equipment providers. And also in this case there may be scarce interest for an

academic researcher.

Nevertheless, the scenario is changing, due to the growing complexity of application boards (telecom, aero spatial, defense, security) and to the market competitiveness: the test engineer experience on the equipments is not enough, and the figure of a Design for Testability engineer should be introduced in order to fulfill the requirements of high quality products, to reduce the number of re-cycles and to shorten the design and production phases (and consequently the time to market). As an example, a further research over the following topics would be of great help for the board DFT engineer:

- an accurate test strategy and planning is required from the initial phase of the board design: very often, one test technique is not enough for covering all defects that may occur on a board, therefore a cocktail of techniques is required, but there are no formalized methods for choosing the cocktail ingredients and pre-calculating the real coverage (no metrics is provided for this purpose)
- learning from ASIC experience, some self test, self-repair and online test may be very useful both for saving test time and for reducing the number of board coming back from the field
- the extension of board test techniques to system test typically is not one of the highest priorities but it might be studied with much more care.

This topic list, of course, is not meant to cover all possible aspects (no limits should be put to researchers' fantasy!) but may give an idea of what a board DFT engineer can dream to learn at ITC in the near future.