

## Board Test: Wanted Dead or Alive

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“Why am I using complicated electrical test methods to discover my mechanical assembly problems?”

That simple question, asked over ten years ago by a manufacturing VP at a leading personal computer company, started significant rethinking about the board test products I was involved with at the time. The question can also help us to understand why board test has almost completely disappeared from the ITC program, despite repeated attempts by Program Chairs and the Program Committee to reinvigorate it.

When I first attended ITC, board test was exciting and challenging. The conventional functional test was under attack by an upstart called in-circuit, which depended on a bed-of-nails fixture and “electronic brute force”. There were several other technologies aimed at the microprocessor-based boards, such as memory emulation, which inserted a tester’s memory into the board’s data paths in place of the board’s boot ROMs. All of these techniques had an emphasis on accurate diagnosis. Some of the board test technology from the 70s and 80s is being rediscovered today by semiconductor DFT, BIST and diagnostic researchers.

Even then we could sense the challenge of dealing with realistic defects: and the board test community came up with its answer: boundary scan. Here was a test technology solution to many of the problems of the existing board test techniques, that clearly addressed the real-world manufacturing defects in a world where the in-circuit fixture could no longer access enough, and where people were disturbed by the damage in-circuit test could cause.

We were so caught up in the excitement of developing the “complicated electrical test methods” that we had forgotten that they might not be the most

effective tools for the real customer problems. And the hard realization that the customers were only really interested in finding “mechanical assembly problems” made us look at new solutions.

One path was “simpler electrical test methods” that were less dependent on information about the components and their characteristics. Another path was to find “non-electrical” inspection tools that could find the same defects. These non-electrical methods had an added bonus: they detected “mechanical assembly problems” such as open power and ground pins that our electrical test methods missed, and could measure feature size variation before it became an actual defect.

But this was hardly ITC paper material. The whole “unpowered opens” set of test methods were never reported in the normal ITC paper process, but only in “Lecture Series” where we invited the developers to present “practical” material. Optical and X-ray inspection of boards has never been covered at ITC.

Is there any future for board test at ITC? I could easily say, “No, it’s a dead topic. ITC should focus on where it excels, which is DFT and semiconductor test”. Instead I’ll give a qualified “Yes, plenty of interesting techniques are used in testing complete boards as systems”. Let’s hear about those techniques now. This is not conventional simulated functional test, but functional test using a variety of realistic environment instruments.

Board test at ITC should not be about complicated ways of detecting mechanical assembly defects, but about ways of detecting subtle interactions in the products so that even when made perfectly, from good parts, they still don’t work. After all, the semiconductor test experts will need to know those methods in ten years time.