

Pervasive Multi Giga Bit links- an ATE challenge?

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The trend lines

The data rates of high-speed serial communications have increased to the point where many communications designers are implementing multilane serializer/deserializer (SerDes) I/O architectures on their highly complex Systems-on-a-Chip. Taking such an approach maximizes the use of limited pins on these devices while enabling ultra high bandwidths at data rates beyond 2.5 Gbits/second for high-speed communications protocols such as Ethernet, Sonet, Infiniband, Fibre Channel and so on.

And trend lines indicate that this multi gigabit link technology is starting to be used across the board. Examples like SATA, HyperTransport, Rapid IO, PCI Express demonstrate the changing landscape in the computation segment. Serial link technology used to be a domain of the “telecom folks”, done in exotic processes and at rather limited volumes, TODAY CMOS has stepped up to the plate, SOC integration has begun. Nevertheless the economic reward is in HVM commodity rather than in the particular I/O technology.

The challenge

General purpose ATE traditionally lags behind in technology and platform evolutions hardly keep up with leading edge technology steps. What is different these days?

The pervasive deployment of high-speed serial link technology presents an extremely high economic pressure. While I/O rates take a steep jump from 500...600 Mb/s in conventional single-ended technology to 2.5 .. 3.2 Gb/s in differential unidirectional technology the test cost budget really needs to be significantly lower than today’s main stream. And the CMOS folks already indicate that they are ready to scale it further. To make things worse the test challenges for SOC designs with embedded serial links are quite substantial:

High-speed serial architectures go hand in hand with the deployment of multiple domains, the challenge of managing non predictable latencies and “non deterministic” pattern streams due domain boundary slips and protocol arbitration.

This puts a big question mark behind the classic “faster, bigger, better” approach of chaining up pin resources.

A review of ATE to deal with these challenges while focusing on the economic equation is at call!

At the same time major efforts are underway in the field of DFT and BIST to help address the design and test challenges. Scan strategies are evolving, I/O wrappers are being deployed, BIST engines are heavily used, but tools also barely keep up with advances in process technology and integration density. Integration density progresses and new failure mechanisms develop making fault modeling an ongoing challenge.

What needs to be done?

The leading theme for manufacturing needs to be: Where do we need to rely on EXTERNAL judgement (ATE), where can DFT/BIST become strong at and how do we COMPLIMENT the solution space at best? For the engineering challenge the theme is different: What do we need to QUALIFY the design for manufacturing, how do we ensure that the DFT/BIST scheme delivers the desired results AND what do we need to QUANTIFY the design margins? The art is making the right trade offs!

From a TEST SOLUTION viewpoint the strategy looks like

- ensure and renew an economic volume production platform as the foundation
- provide engineering capabilities to manage immaturity
- provide qualified instrumentation
- deploy access to leading edge process technology
- actively drive design tool cooperation, active research of methodologies to take DFT and BIST capabilities into the test platform design
- work and learn with leading edge customers
- continuously INNOVATE and CHALLENGE yourself

Combining ENABLING capability and lowest cost of test in a single platform provides customers the highest economic return.