Multi-GHz Interface Devices Should be Tested Using External Test Resources

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1. Problem Statement and Key Measure

Problem Statement. Everyone will agree that a key issue in the design of multi-GHz interface devices is jitter performance. To characterize jitter performance, do you measure timing jitter or period jitter of the device? Should the Bit Error Rate performance of the device also be tested? Is there any way to shorten the overall test time? And as always, is there a way to reduce the test cost? Furthermore, is it appropriate to reduce the equipment cost by partitioning test resources on-chip?

Which Jitter? First, you have to understand what kind of jitter you should measure for testing your device. In the case of high-speed I/Os, the key measure is not a period fluctuation of the clock signal but a timing misalignment between data sequence and clock signal. Therefore, you should measure edge fluctuations (= timing jitter) in both the data sequence and the clock signal. Only the $\Delta\phi$ method can estimate timing jitter directly [1].

Furthermore, a spectrum analyzer measures timing jitter as phase noise spectra in the frequency domain. Note that the most accurate instrument for measuring phase noise or timing jitter is not a time-interval analyzer but a spectrum analyzer, which performs its measurement by sweeping a bandpass filter along the frequency axis. The RMS value of timing jitter is related to the area under the phase noise curve [1]. Thus, the RMS value of timing jitter can be easily calibrated by using a spectrum analyzer.

Secondly, a very different way to perform jitter testing on a production line is needed. Since it sometimes takes 10-20 sec to perform a jitter tolerance test, almost all data sheets of SerDes devices give only a typical value of jitter tolerance. In other words, production line testing is not done. No currently available method can provide a jitter test solution in production test, either on-chip or off-chip. However, a newly proposed method at this ITC enables measurements of both jitter transfer function and timing misalignment simultaneously [2].

2. Test Resource Partitioning for Testing Jitter

Which approach should be used to test these high-speed interface devices: allocate an on-chip test resource or use an external test resource? I propose that external test resources such as ATE be used for testing such high-speed I/Os. Why? Because jitter is very sensitive to the activity of the on-chip circuits. Reference [3] reports that both the deterministic skew and the RMS value of the random clock skew of the "noisy" clocks were nearly two times larger than those of the "quiet" clocks. This means that the activity of the on-chip timing test circuit itself will induce additional fluctuations on edges of the data sequence and the clock signal. This may cause the rejection of good devices.

Furthermore, no method can provide on-chip capability for testing timing jitter. Currently available methods, which are based upon use of non-zero dead-time counters, can only measure period [4]. Here again, very different circuits from current on-chip measuring circuits need to be developed in order to make on chip testing more viable.

3. Summary

We have to test multi-GHz interface devices by measuring timing jitter. This provides us with a shortcut to reduce test time. Furthermore, we can now measure the jitter transfer function and jitter tolerance simultaneously.

External test resources such as ATE or instruments should be allocated for testing such high-speed I/Os. After good correlation between measured values by an ATE and those of an on-chip circuit has been establishing, some tests could be implemented on-chip.

References

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