

The Impact of Outsourcing on Test

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Millions of dollars of technology and engineering go into each new IC product line – be it five dollar chips or five hundred dollar chips. As turn-around times shorten and as IC composition becomes more diverse, it is difficult for any one institution to support the entire creation flow. Thus, parts of the chip creation technology or procedures are increasingly outsourced.

Creating a modern IC is the process of mixing objects and infrastructure from internal and external sources. For example, automation tools, methodologies, IP, cell libraries, fabrication process and manufacturing. In the complete creation flow from specification to delivered package, all of these are forced to interface thus complementing and constraining one another.

Outsourcing black-boxes a part of the chip creation process. In order to compensate for the associated loss of control, it is important to provide a clear and accurate specification of the expected deliverable. To do this and to set the correct expectations, the legacy assumptions and implications concerning the tasks to be replaced must be rediscovered. This is important since some of these are hidden by smooth accustomed practice. In general, methodologies with an established competence are impacted the most.

Sometimes R&D for internal techniques needs to be redirected towards, for instance, incoming quality control and supply chain management. In addition, some valuable internal techniques may need to be abandoned - resulting in a loss of competitive differentiation in these areas. For example, many companies possess decades long investments in internal automation tool sets. These frequently contain advantages not yet available in commercial offerings. Thus, replacing all or parts of an internal platform can introduce gaps in capability. Niche scan methodologies, ESD protection and controlled leakage that are based on libraries, IP or process are also affected in a similar manner.

Disclosing an advanced technique to a supplier may be done so as not to lose an ability, but the competitive nature is still essentially waived. In addition, the user may become over involved in research and development for a supplier or get caught in an extensive beta testing quagmire. The latter is a persistent industry problem with general tool acquisition. Moreover, as suppliers typically wish to address a diverse set of customers, the available level of customization is typically limited or expensive. While it is good to have alternatives to a particular outsourced technology, it is an expensive engineering trap to perpetually customize an external solution. In fact, it can defeat the purpose of buying it.

Standards are important to interfacing internal and various outsourced objects. For instance, when dealing with circuit cores, the absence of test standards implies effort to retrofit the core DFT to interface with that of the host chip. Also, open data standards will aid the user in creating a mixed flow of best-in-class tools from a range of suppliers. In an environment where technology and automation needs changes with product and process, this ability of a methodology flow to react can be a differentiating characteristic.

With outsourcing test and parts of the design, it is critical to recognize that some accustomed skills and advantages will be forced obsolete, and new ones need to be created. Fast diagnosis is an example of the latter. For some chips, outsourced IP and the host chip target the same new process. For volume ramp, it is likely that a complicated IP block will share the same yield (and even turn-on) issues as the host core. Now, however, complete details of the IP may not be known. A simple example is a netlist understood by the user's gate-level diagnosis package. Cooperation with the supplier will be needed. This, however, may be cumbersome. Strong diagnosis capability is also needed for when targeting early access of a new external fabrication process. Essentially, lowered access to real fab-data can force the user to design with successively refined approximations. As artwork release may precede or coincide with process-model stability, testing of skew wafer lots may be needed to verify the design and predict yield. Should errors occur, the speed and precision of diagnosis and repair will determine the success of the early access plan.