

IC Mixed-Signal BIST: Separating Facts from Fiction

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Introduction

The first papers that proposed on-chip mixed-signal built-in self-test (MS-BIST) were published about ten years ago [1]. The first commercial products were announced five years ago at ITC'97 – LogicVision's adcBIST [2] and pllBIST [3]. The latter tests more PLL parameters than most companies do, and everything is done on-chip in 4K gates: stimulus, response analysis, and comparison to limits. However, PLLs are *not* what most IC designers consider mixed-signal functions. Mixed-signal functions are more popularly deemed to be ADCs, DACs, filters, amplifiers, power regulators, mixers, etc..

BIST, by definition, requires on-chip generation of the stimulus, and on-chip analysis of the response, sufficient to produce a pass/fail result or a series of bits that any tester can compare bit-wise to the expected bit values. Many so-called MS-BIST approaches in fact require the ATE to supply the stimulus (analog waveform, or sigma-delta bit stream), or perform some response analysis (DSP, histogram processing, or RMS calculation), especially when >10 bits linearity is being tested.

What are the facts?

No published approach measures all key ADC and DAC parameters (INL, DNL, THD, SNR, SFDR), except perhaps the McGill University approach [4], which requires a DSP and lots of other circuitry, totaling more than 20K gates for the 12-bit version, and taking more test time than conventional ATE. That approach therefore costs more than conventional test, and also appears limited to <16 bits by the non-linearity of on-chip RC filters, power rail coupling, and inability to fully self-test the BIST circuitry.

Mixed-signal designers and test engineers are a skeptical lot, for valid reasons – they have seen that simulations, silicon performance, and economic feasibility are three different things – every new test approach must be proven in simulation, in hardware, and in production. BIST circuit gate area is obviously of economic importance because it increases IC area, but also because IP providers (3rd party or in-house) usually compare the BIST area to the CUT alone, not the whole IC.

For MS-BIST to be technically and economically successful, it must test all key parameters, at-speed, in a test time comparable to that of mixed-signal ATE, with less than 1~2K gates, and permit new types of tests (and higher accuracy tests) to be added post-silicon – presently this is only available in fiction.

For MS-BIST to become fact, it will have to evolve gracefully and gradually from partitioned test resources. New DFT and test methods that minimize on-chip circuitry will be implemented first, and then the on-chip portion will increase as each component of the test circuitry and method is proven in production.

Engineers may say that sometimes MS-BIST is needed on a chip for self-test in the system. MS-BIST at the board/system level is not fiction – it is often required, but it is implemented using the system's DSP, ADC, and DAC; it is rarely necessary to do it on one chip.

Implementing these system MS-BIST approaches on one chip is technically feasible for IC manufacturing test (e.g., using the DSP and DAC to test the ADC), but it typically requires the same test time as conventional testing because the time is limited by the CUT, or it takes *more* time if an ADC can only be tested after the DSP and DAC is tested or if the ADC has the same resolution as the DAC and thus requires more signal averaging.

Unless an IC has enough embedded test resources to facilitate testing the whole IC on a much lower cost tester, or to permit multi-site testing that is otherwise impractical, then test time must be reduced to pay for DFT silicon area (ICs whose die area is pad-limited are an exception).

Conclusions

True BIST for complete test of 8~16 bit ADCs and DACs is presently fiction. The reasons are technical and economic. It appears technically feasible to test most performance parameters for up to 12 bits accuracy, and some parameters beyond 12 bits. However, for an MS-BIST solution to be economically feasible, it must:

- enable testing mixed-signal circuit blocks or ICs in parallel, and provide test time savings greater than the extra silicon cost;
- or enable use of a lower-cost tester whose capital and/or operating cost savings are greater than the extra silicon cost (if the whole chip can be tested on the tester);
- or enable testing a performance that is otherwise untestable, and which must be tested.

[1] M.J.Ohletz, "Hybrid Built In Self Test (HBIST) for Mixed Analog/Digital Integrated Circuits", ETC, 1991

[2] A.Roy *et al*, "High Accuracy Ramp Generation for A/D Converter BIST", ITC, 2002

[3] S.Sunter & A.Roy, "BIST for Phase-Locked Loops in Digital Applications", ITC, 1999

[4] M.Hafed & G.Roberts, "Test and Evaluation of Multiple Embedded Mixed-signal Test Cores", ITC, 2002