Scan and BIST Can Almost Achieve Test Quality Levels

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Abstract

Structural testing with both scan test and Built-in Self-Test (BIST) has proven effective for detecting both gross static and at-speed defects. As tools and techniques improve, structural testing is approaching the high level of test quality necessary to eliminate test escapes. However, scan and BIST do not accomplish all that is needed. Parametric and functional tests are still needed for advanced microprocessor and Systems on Chip (SoC) designs

1 Introduction

This panel will debate the question “Can scan achieve the quality level we are looking for?” Based on data collected for an advanced microprocessor design, my answer is that structural test, including both scan and BIST, is “almost good enough”. This, of course, means that at the current levels of investing in Design for Test (DFT) features, functional tests still have a sufficiently important role to play in test quality.

2 Contributions to Test Quality

To illustrate the importance of each type of test, we analyzed actual fail rate data. We collected detailed tester logs, taken at the wafer probe, for over one million parts of a high-volume microprocessor. Based on a random sample of 10,000 of the tester logs, we calculated the percentage of bad die uniquely failing each type of test. For complete information on the study and the various conclusions of the test, please see [1], which is also being presented at the International Test Conference this year. Table 1 presents the uniquely detected fails for each type of test. Since many defective die will fail more than a single test type, the right hand column does not add to 100%. The table shows the unique contribution of each type of test to test quality.

Table 1: Unique Detection Rates

Test Type in Order of Execution	% of Bad Die Uniquely Detected
Continuity	3.16 %
IDD Trip	23.32 %
IDD Static	0.00%
Leakage	1.26 %
DC Levels	0.00 %
Memory BIST	3.89 %
DC scan	14.70 %
AC scan	2.81 %
DC scan and AC scan	16.95 %
JTAG	0.40 %
Functional	6.21 %

While most tests were run whether a fail was detected or not, please note that if a die failed either Continuity or IDD Trip tests, the remaining tests were not run. This results in these tests appearing to have a higher impact on uniquely failing the die than would actually be the case. Most if not all of the other test types would fail also. In the case of the AC Scan test, if DC scan tests failed, then the AC scan tests were not run. Since both AC scan tests and functional tests detect at-speed defects, this also inflates somewhat the ability of functional tests to uniquely detect bad die. Since the ATPG tools do not yet do a good job generating patterns to detect at-speed defects around custom embedded memories, functional patterns are required for coverage.

Despite the minor caveats on what the statistics reveal, it is clear that memory BIST, DC scan, and AC Scan detect the majority of bad die.

Of course, since we have a strong DFT content in the design, we have not attempted to have a truly exhaustive functional test suite. The generation and application such a test program would be very costly. Instead, the functional tests are generally targeted to cover areas that we know are not well covered by the structural tests. These areas include design features such the different bus configurations, custom circuits such as the PLL and speed sensitive paths.

3 Conclusions

Collectively the structural tests are the most important class of the tests for test quality. While the DFT effort requires a significant investment, we simply could not meet the Time to Market requirements with only a functional test approach. Yet despite the high test effectiveness of the structural test patterns, they are still truly are not enough to meet the required test quality. We rely on functional patterns for some test coverage and as the primary method of speed-binning the processors. Therefore, until the industry tools improve, scan and BIST can only get us most of the way to total test quality.

4 References

1. J. Gatej, L. Song, C. Pyron, R. Raina, T. Munns, “Evaluating ATE Features in Terms of Test Escape Rates and Other Cost of Test Culprits”, *International Test Conference,* 2002.

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