Inevitable Use of TAP Domains in SOCs

Lee Whetsel
Texas Instruments

The 1149.1 TAP controller has proven to be an effective test interface for ICs on boards using its standard 4 pin interface (TCK, TMS, TDI, TDO). One of the most important features of the TAP is its Protocol, which provides an easy to follow Plug & Play IC test interface. This Protocol defines and enforces; (1) a Test Reset Mode, (2) a Run/Test Idle Mode, (3) an Instruction Scan Mode, and (4) a Data Scan Mode. IC level IEEE standards that currently use the TAP Protocol include; IEEE 1149.1 (the Boundary Scan Standard), IEEE 1149.4 (the Mixed Signal Test Bus Standard), IEEE P1149.6 (a proposed Advanced Digital Interconnect Test Standard), IEEE 1532 (an In-System Programming Standard), and IEEE 5001 (a Silicon Debug Standard) . Further, numerous companies/consortiums use the TAP protocol at IC level to support various silicon debug, emulation, and code development strategies. As these users of TAPs migrate their products from individual ICs to reusable IP Cores, it appears inevitable that Systems-on-Chip (SOC) will include more and more embedded TAP domains.

Some of the concerns to using multiple TAP domains in SOCs include; (a) embedded TAP domains are not compliant in an IC level 1149.1 architecture, (b) the TAP is a serial test interface and thus slow, (c) the TAP Protocol is too rigid and does not provide test control flexibility, and (d) the TAP is not testable. Reference 1 provides one example solution for concern (a) and is based on insuring that following power up or a test reset only the IC's TAP domain (IR and DR architecture) is coupled between TDI and TDO. Reference 2 provides one example solution for concern (b), and is based on using an 1149.1 test instruction to enable a parallel test access mechanism facilitating parallel scan testing. Reference 2 also provides one example solution for concern (c) and is based upon using an 1149.1 test instruction to remove dead states from the TAP to allow the TAP to provide conventional scan test control of internal scan paths. Reference 3 provides one example solution for concern (d) and is based on designing TAPs with self-checking capability.

The IEEE P1500 Embedded Core Test Standard is defining a core test Wrapper architecture. The test Wrapper architecture is similar to the 1149.1 boundary scan architecture with the exception that a TAP is not used to access to the Wrapper's instruction and data registers. P1500 also is defining instructions for enabling parallel test access mechanisms to be coupled to the core via the Wrapper to allow higher test data input and output bandwidth to and from the core. A user of P1500 may add a TAP to the Wrapper architecture if it is desired to link the P1500 domain up with other TAP domains residing in an SOC. One key advantage of using a TAP'ed P1500 Wrapper is that serial instruction and data loads to P1500 domains would be Plug & Play compatible with serial instruction and data loads to other embedded TAP domains. The execution of a test instruction loaded into a TAP'ed Wrapper does not need to be controlled by the TAP, but rather it could be controlled by a test control interface enabled by the loaded test instruction. Thus in one example of implementation, a Wrapper may include a TAP for Plug & Play instruction loading, while allowing execution of the instruction to occur from control separate from TAP control.

References
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2 – Maunder, Chapter 18 of The Test Access Port and Boundary Scan Architecture, 1990 IEEE Computer Society Press Order # 2070.
3 – Mitra, McCluskey, Makar, Design for Testability and Testing of IEEE 1149.1 TAP Controller, pages 247-255, 2001 IEEE VLSI Test Symposium.

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