TAPS all over my chip! So now what do I do?

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The Test Access Port (TAP) and associated controller, standardized in IEEE Std. 1149.1, is often used to control a wide variety of functions. For example, several existing cores use the TAP and associated controller to control internal test (e.g. Logic-BIST) and debug (e.g. scan dumping) functionality.

It is also common to see multiple of these cores, each with their own TAP controller, integrated on a single system chip. When this happens, a means of chip-level access needs to be created to be able to use each TAP controller to test or debug the corresponding core. Preferably we do not want to introduce a separate TAP port on the system chip for each internal TAP controller as this can quickly lead to an excessive number of device pins dedicated for test and debug, which is very costly.

A solution to this problem is presented in detail in Session 3.1, titled “IEEE 1149.1-compliant Access Architecture for Multiple-Core Debug on Digital System Chips”, by Vermeulen, Waayers, and Bakker.

During the verbal position statement, a summary will be given of the reasons why this particular multi-TAP architecture has been standardized within Philips Semiconductors after more than a year of investigation.

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