

CAN IC TEST LEARN FROM HOW A TESTER IS TESTED

Rochit Rajsuman

Advantest America R & D Center, Inc.

3201 Scott Boulevard

Santa Clara, CA, 95054

A tester as well as IC is a system at different abstraction levels. The testing of each of these systems should contain individual component testing as well as a full system level functional test to ensure its functional correctness.

In Ref [1-2], an event tester was described. The main attributes of event tester are that it uses vectors directly from the design simulation (vcd); thus, it avoids vector conversion processes and allows event edit/manipulation for test/debug. The implementation of event tester required all new hardware as well as whole new tester software. The hardware design included a new ASIC, design of new pincard, motherboard and backplane as well as a new testhead, hifix and loadboard. The software design included a new compiler, a new middleware, a new application server, a new kernel and a new user's interface.

Component Testing

The test methodology for new ASIC of event tester consisted of functional, structural, memory and Iddq test. The structural test methodology is full scan design with JTAG. For embedded memory, direct access and external testing was used using a 9n March algorithm. All of these tests were supplemented by an Iddq test.

The pincard tests included functional test and connectivity tests. The board manufacturing test consisted of initial raw board testing, followed by the testing of completely assembled board. The assembly quality assurance also contains full visual inspection and random spot x-ray examination.

The software components were checked for compilation error, linking error, run exceptions, halt on any asserted statements used by the designer for error detection and that it pass all its unit tests. This methodology included functional coverage, line coverage and checks for memory leaks. The functionality of each component was tested by unit tests.

A tester simulation model was developed, which could be installed on a desktop computer and function like a full functional tester using an IC simulation model. Using this simulation model and manual targeted tests, a number of objectives were achieved that include (i) testing the operation of

each function in integrated environment; (ii) check the minimum and maximum limits of the operation for each function; (iii) usage consistency; (iv) error handling by the integrated system for incorrect data entry; (v) overall speed and response time of the software; (vi) accuracy and consistency of data display. In addition to the targeted tests, random tests were used to activate obscure part of the software that was difficult to exercise by normal operation.

Functional Testing

The initial testing of the full system included targeted and random tests with both hardware and software diagnostic routines. The full test routines are designed to check all connectivity as well as full testing of components, i.e., event memory, ASIC, pin electronics including AC/DC levels, PMU etc.

The full functional testing of this tester consisted of calibration of all test channels and operation of the system over a wide range of temperature and voltage variations and system power configurations. After full system diagnostics and calibration, the whole machine was subjected to real world tests using a number of known good and bad ICs. Our first test case was our own ASIC that was developed for this system. The second test case for this tester was SUN Microsystems MicroSPARC-IIep microprocessor. These two cases provided preliminary testing of the overall system; an additional set of designs being used to explore and test all aspects of this tester.

What Can IC Test Learn

IC test can follow the same path. All individual blocks can be tested as individual components. A full functional test of IC should be done regardless of the fault coverage of individual blocks and test methodology including DFT, structural test, Iddq etc. The interfaces and synergy in the operation of blocks can only be determined by functional test.

References

1. J. Katz and R. Rajsuman, "A new paradigm in test for the next millennium", Int. Test Conference, pp. 468-476, 2000.
2. R. Rajsuman, "Bringing test to design: testing in the designer's event based environment", Int. Semi Technology Symp, Semicon West, 2002.