

Test Coverage Models for System Test?

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In the world of IC testing, efficiency measurements are based on test coverage of modeled faults, often stuck at faults. While this has been effective at the chip level to improve the quality of chip testing, the question is how can this be transferred to the system test level?

At the system level we are faced with several potential complications in measuring the quality of the test process. These include the fact that all of the chips have already been tested individually and tested again when they were put on the board. This previous testing leads to a vague fault spectrum and a non-random fault distribution. Do we count the supplier test coverage in the overall system test coverage? Multiple suppliers with different levels of test coverage and quality for the same component can also complicate the determination of test coverage. System configuration options can vary widely within one system type. These complexities need to be dealt with while keeping any test coverage analysis simple enough to explain to management and other stakeholders. The author will discuss two possible techniques to address these complications. In the first technique, we will look at what a comprehensive fault model may look like at the system level. The second technique involves a more traditional approach of implementing a test coverage analysis based on functional faults and Failure Mode Effect Analysis (FMEA).

The first possibility is an extension of the IC test techniques. If each supplier to a system creates a standard data set with the key information for modeling fault coverage, then we could simulate our test process against the model with each component resulting in a test coverage output. The question becomes what level of detail would be required, and how useful would it be?

In order to do it correctly, we need a level of detail that included the chip, board, and system level faults. So the model would need to be at least three tiered. The model would need some methodology for dictating fault definition, probability, and knowledge of when the faults are activated. The usefulness of this model simulation depends on the accuracy of the simulation,

which in turn requires a data collection process that is accurate enough to get the fault definitions and probabilities correct.

The second solution gets around the complexity issues by generalizing the faults spectrum into functional faults. This has four advantages. Functional failures align test coverage with field issue descriptions. It simplifies fault insertion and test development. It is easy to understand for management. Functional testing is usually portable across different suppliers of the same product.

Using an FMEA approach we would perform a risk analysis on each component of the system. For each function of the component, this involves looking for failure mechanisms that include supplier test escapes, system interaction issues, physical damage, and early life failures. The probabilities associated with these failure mechanisms are estimated via supplier test coverage, failure analysis, and engineering expertise and verified with factory and field data collection. The data collection can be fed directly into the model to keep it reasonably accurate. The effect of each risk will then be assessed based on the impact of the failure to the customer. By combining the probability with the effect of the fault, it can be categorized as high, medium, or low risk to the customer.

The final step is documenting what percentage of the possible failures the system test process covers. For example, the tests may cover 100% of the high-risk faults, 98% of the medium risk faults, and 95% of the low risk faults. Management and other stakeholders can understand what the known test escapes are since the risks are related to functional failures.

Either of these techniques or some combination of both should allow for a reasonably accurate measure of test coverage. The second solution is more preferred until better fault models are defined for the system test environment. Further fault modeling research should target system interaction faults, connectivity faults, and infant mortality faults.