

# TESTING THE TESTER

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The end use of a tester is to test ICs; hence, it is imperative that the tester itself should function correctly. A broad strategy is employed to detect and remove component level faults from various hardware and software components. Furthermore, a system level test methodology is used to ensure full functional correctness of the tester.

In Ref [1-2], an event tester was described. The main attributes of event tester are that it uses vectors directly from the design simulation (vcd); thus, it avoids vector conversion processes and allows event edit/manipulation for test/debug. The architectural difference from cyclized ATE is shown in figure 1. The implementation of event tester required all new hardware as well as whole new tester software. The hardware design included a new ASIC, design of new pincard, motherboard and backplane as well as a new testhead, hifix and loadboard. The software design included a new compiler, a new middleware, a new application server, a new kernel and a new user's interface.

accuracy and consistency of data display. In addition to the targeted tests, random tests were used to activate obscure part of the software that was difficult to exercise by normal operation.

The initial testing of the full system included targeted and random tests; both hardware and software diagnostic routines were employed to determine the cause of error. Hardware diagnostic routines were designed to localize the error on a pincard and to its specific component, while software error messages were designed to identify a specific software component or interface. Specific diagnostic routines were developed for our diagnostic (tester manufacturing diagnostics) as well as diagnostics from the end-user point of view. The routines in each of the group can further be categorized as (i) quick test; (ii) full test.

The full test routines are designed to check all connectivity as well as full testing of event memory, ASIC, pin electronics including AC/DC levels, PMU etc.

The full functional testing of this tester consisted of calibration of all test channels and operation of the system over a wide range of temperature and voltage variations and system power configurations. Advantest has a specialized calibration robot that measures various pin parameters over a specified voltage and temperature range.

After full system diagnostics and calibration, the whole machine was subjected to real world tests using a number of known good and bad ICs. Our first test case was our own ASIC that was developed for this system. The second test case for this tester was SUN Microsystems MicroSPARC-IIep microprocessor. These two cases provided preliminary testing of the overall system; an additional set of designs being used to explore and test all aspects of this tester.

## References

1. J. Katz and R. Rajsuman, "A new paradigm in test for the next millennium" Int. Test Conference, pp. 468-476, 2000.
2. R. Rajsuman, "Bridging test to design: testing in the designer's event based environment", Semi Technology Symp, Semicon West, 2002.

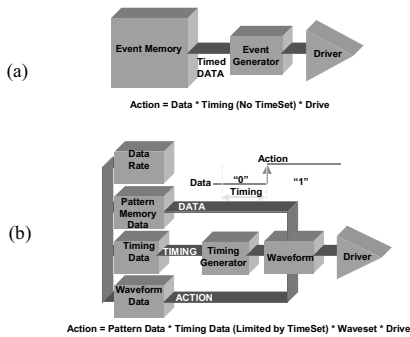


Fig. 1: Tester architectures: (a): Event tester architecture; (b) Architecture of cyclized ATE.

A very intensive task in functional testing was system simulation with targeted and random tests. A tester simulation model was developed, which could be installed on a desktop computer and function like a full functional tester using an IC simulation model. Using this simulation model and manual targeted tests, a number of objectives were achieved that include (i) testing the operation of each function in integrated environment; (ii) check the minimum and maximum limits of the operation for each function; (iii) usage consistency; (iv) error handling by the integrated system for incorrect data entry; (v) overall speed and response time of the software; (vi)