Homegrown Tools and Equipment versus EDA and ATE Vendors: Future of Design to Test Product Lines

Dale Hoffman
IBM, Electronic Design Automation

Summary Statement

Tight integration of EDA tools and design methodologies with fabrication equipment and manufacturing processes is a key success factor for leading-edge semiconductor technology companies. In particular, the ownership of methodologies and processes to a large extent controls how well new technologies can be rolled out and ramped up to production. Ownership of test-related design, manufacturing, and engineering software systems enables superior ability to quickly adopt relatively generic equipment hardware platforms to the rapidly changing technology requirements. Keeping the core software systems development in-house makes it easier to deliver and deploy the right tools and methodologies for industry-leading technology innovations, like copper interconnect or SOI, before those technologies become commonplace. A good example of the strength of in-house synergy between tool and methodology development is the highly automated vectorless sign-off flow for IBM's ASICs.

For the future we foresee a further growth in importance of test-related software systems. Both, the complexity of the product designs and the complexity of the process technologies, drive the need for even tighter integration between Design For Test (DFT), Design For Manufacturing (DFM), production test control/management, and diagnostics/failure analysis. Automated Test Equipment (ATE) has to evolve towards more flexible, open hardware and software architectures that allow for rapid re-configuration with a variety instruments that are able to collect a wider range of manufacturing data. We anticipate that data from multiple test stages will be collected and processed by equipment-neutral analysis software systems. These software systems, not the ATE, will make pass/fail and binning decisions, modify the test/screening flow where appropriate, and provide rapid feedback for process control and yield learning. The increasing DFT content of leading-edge SoC chips demands new software infrastructures that make the chip-specific DFT content accessible and useable by test and design engineers on multiple test and debug hardware platforms.

0-7803-7542-4/02 $17.00 © 2002 IEEE