

## **Homegrown Tools and Equipment versus EDA and ATE Vendors: Future of Design to Test Product Lines**

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The escalation in test cost has been given a great deal of attention recently and several approaches have been pursued to alter test strategy to lower cost - of - test. The large independent device manufacturers are replacing the requirement for every increasing frequency, accuracy and pin count in their ATE equipment with design-for-test (DFT) solutions. This approach may be successful for high volume products but it does not solve the cost problem for the industry.

Circuit complexity is rising. With the introduction of SOC and SIP circuits MEMS, optoelectronic components, sensors as well as a wide variety of traditional circuit fabric types are combined in a single package. ATE vendors will not provide the necessary specialized instrumentation required to test all these elements in the time frame needed. EDA systems must incorporate co-design of circuits, packages and test strategy if the dual “market imperatives” of shorter time-to-market and lower cost-of-test are to be met. The only practical solution is an open architecture allowing any designer of a specialized component to design the necessary instrumentation with its use enabled by the infrastructure of Open Architecture ATE. Both the ATE architecture and the EDA systems must enable test strategy partitioning between BIST, other DFT approaches and traditional ATE. The closed architectures and one dimensional EDA tools that dominate the landscape today will not be viable tomorrow.

The only cost effective way to bring these technologies to bear on test problems is to enable them through co-design and open architecture. This architecture must incorporate:

- Industry standard bus structure
- Compatibility with all relevant industry standards
- Browser technology to access and control resources
- Component structure to enable reconfigurability
- Partitioned test capability in both the EDA and ATE systems

Summary:

- Test cost will drop dramatically on a per transistor basis over the next 3 years
- Device and test co-design will be enabled to allow efficient partitioning of test
- Time-to-market delays associated with test will reduce by an order of magnitude
- Open architecture EDA industry standards will emerge that support insertion of home grown components
- New companies will emerge and take share if the current leaders do not recognize and take advantage of this transition.