The Heisenberg Uncertainty of Test

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As integrated circuit geometries become smaller, distinguishing good parts from bad is becoming increasingly difficult. Quantum mechanical effects such as tunneling are becoming more evident, affecting leakage and reliability, amongst others. As the variance of circuit parameters increases, it is becoming progressively more difficult to retain only traditional tests, which for digital circuits, base passing or failing on what are effectively fixed thresholds: is the output the correct logic one or zero?

I_{DDQ} testing was one of the first approaches where parameter variance caused a fixed threshold approach to break down, and required more sophisticated approaches, frequently statistically based. Defect-based test has developed methods based on the fundamental question of "which ones are different", rather than "which ones are bad"? Limits are set by examining population statistics and determining outliers based on statistical metrics such as standard deviation. To capture outliers, a wider range of test variables needs to be used, such as voltage, frequency, temperature and die location.

As CMOS continues to evolve, parameter spread is increasing, posing significant challenges to detecting outlying parts, particularly when the range of test variables is becoming more limited. For example, available voltage acceleration for burn-in is becoming much less, making this traditional reliability screen less effective. In a world of distinguishing differences in a broad population, are we approaching the "Heisenberg uncertainty" of test? We can tell which parts are different but not how they differ, or how parts should differ but not which parts they are.

In response to the CMOS issues, which include cost as well as test, there has been significant effort devoted to developing alternative technologies such as nanotechnology. Although there are still technical hurdles to be overcome, approaches such as molecular electronics offer potentially attractive solutions. Here quantum mechanics must be dealt with, and it is interesting to discuss test problems in such technologies. Defect tolerance will be essential and it is quite possible that the present day costs which prevent defect tolerance in random logic will change due to the huge level of integration possible at the molecular level.

Invited Address

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About the Speaker

Dr. Maxwell received his Ph.D. from the Australian National University. He works in Agilent's Semiconductor Products Group in the area of DFT, test methodologies and test effectiveness. He received the ITC 1991 Honorable Mention Award for work on test methods effectiveness, and his work in I_{DDQ} test received the ITC 1999 Best Paper Award.

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