

Plenary Speech 2P.3

Performance Limitations of Devices and Interconnects and Possible Alternatives for Nanoelectronics

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For over three decades, there has been a quadrupling of transistor density and a doubling of electrical performance every 2 to 3 years. Si transistor technology, in particular CMOS has played a pivotal role in this. It is believed that continued scaling will take the industry down to the 35-nm technology node, at the limit of the "long-term" range of the International Technology Roadmap for Semiconductors (ITRS). However, it is also well accepted that this long-term range of the 70-nm to 35-nm nodes remains solidly in the "no-known solution" category. The difficulty in scaling the conventional MOSFET makes it prudent to search for alternative device structures. This will require new structural, material and fabrication technology solutions that are generally compatible with current and forecasted installed Semiconductor Manufacturing. In addition, new and revolutionary device concepts need to be discovered and evolved. These can be split into two categories: one is the continued use of silicon FET-type devices but with additional materials, e.g., Ge and innovative structural aspects that deviate from the classical planar/bulk MOSFET, e.g., double gate MOSFET. The second category is a set of potentially entirely different information processing and transmission devices from the transistor as we know it, e.g. silicon-based quantum-effect devices, nano-tube electronics and molecular and organic semiconductor electronics. Continuous scaling of VLSI circuits can pose significant problems for interconnects, especially for those responsible for long distance communication on a high performance chip. Our modeling predicts that the situation is worse than anticipated in the ITRS, which assumes that the resistivity of copper will not change appreciably with scaling in the future. We show that resistance of interconnect wires in light of scaling induced increase in electron surface scattering, fractional cross section area occupied by the high resistivity barrier and realistic interconnect operation temperature will lead to a significant rise in the effective resistivity of Cu. As a result both power and delay of these interconnects is likely to rise significantly in the future. In the light of various metal interconnect limitations, alternate solutions need to be pursued. We focus on two such solutions, optical interconnects and three-dimensional (3-D) ICs with multiplicative Si layers.

About Krishna Saraswat

Prof. Saraswat received the B.E. degree in Electronics and Telecommunications in 1968 from Birla Institute of Technology and Science, Pilani, India, and the M.S. and Ph.D. degrees in Electrical Engineering in 1969 and 1974 respectively from Stanford University, Stanford, CA. During 1969-70, he worked on microwave transistors at Texas Instruments, Dallas, Texas and since 1971, he has been with Stanford University, California, where presently he is a Professor of Electrical Engineering and Associate Director of the NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing. During 1996-97 he was the Director of the Integrated Circuits Laboratory at Stanford. Since Dec. 2003 he is also an Adjunct Professor at the Birla Institute of Technology and Science, Pilani, India. Prof. Saraswat has authored or co-authored over 400 technical papers, of which six have received Best Paper Award. He is a Fellow of the IEEE, and a member of both The Electrochemical Society and The Materials Research Society. He received the Thomas Callinan Award from The Electrochemical Society in 2000 for his contributions to the dielectric science and technology. He is the recipient of the 2004 IEEE Andrew Grove Award for seminal contributions to silicon process technology.