

Plenary Speech 1P.2

Design for Manufacturing? Design for Yield!!!

Tuesday, March 23

9:15am-9:45am

Marc Levitt

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Today's nanometer-scale designs are two orders-of-magnitude more complex than designs were in the early 1990s and are commonly manufactured with processes at or below the 130nm feature size. This has brought about a fundamental change in the way design teams must approach the release for their design data to their manufacturing partners. In the past, once a design was taped out and proven to be functional, the responsibility for ramping yield and enhancing the profitability of a design was primarily the responsibility of the manufacturing partner. This is no longer possible at 130nm and below. Once a manufacturing process has stabilized, direct action must be taken by each and every design team to "tune" their design for yield. Design-specific yield enhancement is the new frontier in EDA and while it includes the traditional Design for Manufacturing (DFM) technologies, it also covers much more. Failure to consider yield-degrading effects in IR drop, signal integrity, electro migration, and process variation will result in severe downstream problems in timing closure, functional errors during system bring-up, and the inability to achieve silicon yield and quality targets. In this talk Marc Levitt will discuss what is needed in a new generation design-for-yield tool suite to address the quality of silicon at its source.

About Marc Levitt

Dr. Marc Levitt is the platform vice president of design for manufacturing at Cadence Design Systems. Dr. Levitt came to Cadence in 2002 as product line vice president of design for manufacturing. He then moved into the role of vice president of research and development for nanometer analysis and verification and design for manufacturing at Cadence. Before joining Cadence, Dr. Levitt served as director of VLSI at Transmeta, director of silicon development at Sonics and senior hardware manager at Sun Microsystems. He's also held numerous technical positions at Hewlett-Packard and Digital Equipment. In his professional career, Dr. Levitt has brought up four process nodes and three fabs from 0.5um CMOS to 130nm. He has been published in more than 30 publications. In 1996, he received the Sun Microsystems Engineering Excellence Award. Dr. Levitt earned his master of science degree in electrical engineering, as well as his doctorate in electrical engineering, from the University of Illinois. He also earned a bachelor of science degree in computer engineering from Lehigh University.