

Part 3

Manufacturability

Presenter: **Professor Andrew B. Kahng**, University of California, San Diego

This portion of the tutorial reviews physical design complications and methodology changes – for example, in the detailed routing arena - that arise from sub-wavelength lithography and deep submicron manufacturing (antennas, metal planarization and mask-wafer mismatch). In addition, yield-constrained optimizations in PD are covered, especially “beyond corners” approaches that escape today’s pessimistic or even incorrect corner-based approaches. We also discuss current and near-term prospects for the overall design-to-manufacturing PD methodology. Key aspects include better integrations with analysis and manufacturing interfaces, as well as cost-benefit tradeoffs for “regular” layout structures that are likely beyond 90nm, cost optimizations for low volume production, and the role of robust and/or stochastic optimization in PD.

Part 4

Low-Power Design

Presenter: **Professor Kaushik Roy**, Purdue University

This section of the tutorial will present technology scaling and its impacts on dynamic and static power dissipation. Both leakage and dynamic power estimation and design techniques to reduce power dissipation in scaled technologies will be described.

Part 5

Coping with Uncertainty

Presenter: **Nagib Hakim**, Intel Corporation

Uncertainties from process variations, tool and model inaccuracies, as well as operating environment limit the designers ability to accurately predict product performance and power consumption. Understanding and modeling these effects would enable the development of strategies to better optimize these circuits and perform the desired power-performance tradeoff. The presentation will discuss various sources of uncertainty, their modeling, their impact on various types of circuits, and their use in product development and optimization.