

# ISQED Tutorials

## Compact Modeling and Analysis for Nanometer-scale CMOS Design

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### Part 1

#### **Nanometer-Scale CMOS Devices**

Presenter: **Kerry Bernstein**, IBM T.J. Watson Research Center

This part of the tutorial will examine the operation and idiosyncrasies of emerging deep submicron CMOS devices and materials appearing in future high speed logic products. These novel structures include ultra-thin and fully depleted silicon-on-insulator devices, double-gated transistors, strained silicon, and crystal re-oriented MOSFETs. Molecular computing technologies, such as carbon nano-tubes, and new materials which extend scaling, such as high-k dielectrics, will also be explored. Circuit design issues, soft error vulnerabilities, defect mechanisms and required device model accommodations will also be discussed.

### Part 2

#### **Interconnect Modeling**

Presenter: **Professor Jeff Davis**, Georgia Tech

This tutorial will review compact VLSI interconnect models for both parameter extraction (e.g. R, L, and C) and key transient waveform characteristics (e.g. time delay, crosstalk, and overshoot). The tradeoff between model simplicity and accuracy will be explored by comparing the results of these compact models to more detailed interconnect simulations. The impact of the variability of interconnect layout geometries on the accuracy of these compact models will also be discussed. In addition, these compact models will be used to analyze a variety of VLSI interconnect circuits and structures. This analysis will include an overview of the impact of embedded low-k dielectrics on time delay and crosstalk, time delay optimizations with non-ideal repeater placements, interconnect device optimization with coplanar shield lines, and the impact of repeater insertion on inductive crosstalk.