

Plenary Speech 1P.3

Quality Challenges of the Nanometer Design Realm

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It is commonly agreed that sub-nanometer design is electronic design technology's next big challenge. With the economic stakes higher than ever, the vendors of electronic design solutions must put themselves into their customers' shoes through comprehensive, high-quality programs. My understanding of the differences designers face at geometries below 100 nanometers has led to my discussion of some of the challenges the industry faces in the sub-nanometer realm. This includes the domination of wires in digital design, which requires the ability to design the best quality wires through continuous convergence, a wire-centric methodology. In the nanometer world, the front-end and back-end disappear, leaving the prototype as the chip. This includes detailed wiring, and a new full-chip iteration every day. Most sub-nanometer ICs and SoCs will be digital/mixed-signal. This leads to custom design issues, such as integrating sensitive circuits with massive digital and mixed-signal design, productivity and foundry interface. Nanometer SoC verification includes digital, analog and software, and a 70 percent silicon re-spin rate because of associated functional errors. At sub-nanometer levels, design-in becomes a major bottleneck, especially across a design chain, which can only be solved by silicon-package-board co-design.

About Ted Vucurevich

Ted Vucurevich serves as a Cadence Senior Vice President, reporting to Ray Bingham, President and CEO. He is responsible for driving advanced technology development and directing Cadence Laboratories. In addition, he serves as an executive fellow. Vucurevich co-leads the Strategic Technology Office with James Hogan. The STO researches, plans and promotes a world class Cadence technology roadmap and vision to Cadence employees, customers, and analysts. As director of Cadence Laboratories, Vucurevich represents Cadence on various external boards and interfaces between research efforts and product development. In his prior role as chief architect at Cadence, Vucurevich helped develop the strategies and technology initiatives in system-on-a-chip (SoC)-based design, DSM infrastructure, software interoperability, design methodology development, and Internet-based electronic system design. Vucurevich joined Cadence in 1992 as director of the Analog Physical Design group. In 1994 he was promoted to work as an architect in the Viper Development group. He was later named chief architect and held that position for five years. Prior to Cadence, Vucurevich worked 14 years at Analog Devices where he held roles in product, design and computer aided design (CAD) engineering. He was a co-founder of the Linear Signal Processing Division, where he was responsible for the implementation of a complete mixed-signal ASIC CAD environment. Vucurevich received his BS degree in electrical engineering from the University of Arizona.