

Plenary Speech 1P.1

Platform Leadership in the Ambient Intelligence Era

Tuesday, March 25

8:45am-9:15am



Bob Payne

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Design reuse has become essential to cope with the ever-increasing design complexity. IP level reuse alone has proven insufficient. Platform based design allows the validation of a robust combination of IP blocks and provides a reference HW and SW baseline which can be supported with an integrated development environment. Several years ago we transitioned into the streaming data era with most systems serving as content generation appliances, content consumption appliances or content distribution equipment. Now we have entered the age of ambient intelligence where the streaming data is served up through wireless links. What will platform leadership look like in this new era? How will the SoC infrastructure change as we move to 90nm technology with more than 30M gate per square centimeter integration capacity? How are usage patterns changing and what represents the killer application that enhances the users quality of life by enabling more advanced interaction with the ambient intelligence? What is it going to take to make a step function improvement in system level design productivity? What happens when power optimization becomes the dominant design consideration? What about SoC affordability? What will the SoC design of the future look like? These are just some of the thought provoking issues that will be addressed in Bob Payne's keynote.

About Bob Payne

Bob Payne joined Philips Semiconductors by way of the VLSI Technology Inc acquisition in early 1999. Bob had joined VLSI in October 1989 after 21 years with Honeywell in IC Design and CAD Management roles. His initial assignment in VLSI was as manager of the Technology Centers in the South and Central portion of the US. After that, Payne was manager of graphics development for VLSI's PC Products division. Then from 1992 through early 1997 served as Chief Technical Officer with responsibility for the ASIC Core Technology. Payne then took on the assignment of leading VLSI's design reuse IP development and the VLSI Velocity™ new design paradigm based on the Rapid Silicon Prototyping concept. After VLSI's acquisition Mr Payne is continuing this work on the advanced design process through a thrust we call "System ASIC Technology" and serves as the US CTO in a guardian role for Philips CTO employees based in the USA.

Payne holds an MBA from the College of St. Thomas, St. Paul, Minnesota, a BSEE and MSEE from the University of Minnesota, Minneapolis.