Evening Panel Discussion*

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6:30 pm

Is Quality a Design Constraint for Sub 100nm Designs?

Moderator
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EETimes

Organizer
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Description

Deep sub-micron design (below 100nm) present a number of new design challenges. These include very high masking costs, new interconnect materials and parasitic phenomenon, significant re-engineering at the device level due to changes in basic device performance, very high gate count and pin count designs, complexity in high pin count packaging & test, and finally reduced product life in the marketplace do to the rapid rollout of new technologies. One of the trade offs that is taking place in the industry to address these issues is the decision toward “design existence”, which is the selection of the “first functional implementation” of a design, over “design quality” which is the selection of the “optimal implementation” of a design.

This panel will discuss the trends in the issue with respect to the re-targeting of the design quality issues from the SOC level to the flow and device levels and the impact on this “shift” on the manufacturability of the resulting designs. Issues discussed will include the use of pre-tested IP as a quality metric, the coverage and quality of the EDA design and validation tools, the correlation of these metrics to the actual manufacturing process and the impact of post fabrication process steps (packaging, test, etc) on the yield of the resulting design.

Panelists

Callen Carpenter – President and CEO, Silicon Metrics Corporation
Paul Kempf – CTO and VP Engineering, Jazz Semiconductor, Inc
John Kibarian – President and CEO, PDF Solutions, Inc.
Dennis Monticelli – Fellow at National Semiconductor, Inc.
Resve Saleh – NSERC/PMC Sierra Chair Professor, UBC Vancouver
Norm Towson – President and CEO, Netcell Corp.

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Panelists Statements

Callan Carpenter, President and CEO, Silicon Metrics Corporation

The panel topic starts with the premise that earliest functionality and circuit optimality are mutually exclusive goals. Perhaps, but isn't this exactly the riddle that the successful chip companies of the future must solve? Functionality is not hard to define, assuming a well-written spec. Optimality is a slippery issue; optimum does not mean achieving the theoretical limit of performance for every aspect of a chip. We contend that "optimum" means achieving "good enough" on all technical requirements while staying within the market-imposed constraints of schedule and cost.

At one time the standard chip development schedule included a "time to market" tape out followed by a cost-reduction redesign. While this formula may still work for some markets, many applications have such short life cycles that the first working silicon must also be profitable silicon – there is no time for another spin.

If this is the case, then where lays the onus for ensuring quality (i.e., yield) of the design: the IP providers or the chip integrators? The answer, of course, is both. By mating rigorous methodologies with advanced tools and well-qualified IP, chip designers have the technologies they need to produce functional and profitable chips. A key component to both advanced toolsets and quality IP is an accurate, comprehensive and efficient set of electrical and functional models. Such models enable designers to get the most out of their leading-edge design environment and to validate that their IP building blocks deliver the quality and performance required to get the job done.

Paul Kempf, CTO and VO Engineering, Jazz Semiconductor

As a manufacturer of UDSM wafers, yield as a metric of quality is of highest importance. The complexity of the masking processes and the large of steps involved in the fab cycle, make "existence only" not a sufficient criteria for design. The ROI for the resulting products has to be based on multiple manufacturing runs in a production environment, there are no monetary winners in the multi-project shuttle programs.

The SOC designer, as well as the IP provider and the tool flow specialist are required to understand the technical aspects of the design so that the mfg portion in free to deal with JUST process details knowing that the design being brought up is manufacturabel. The responsibility rightfully ends up belong to the SOC designers and thier IP.

John Kibarian, President and CEO, PDF Solutions, Inc.

The manufacturing yield of deep sub-micron ICs becomes more difficult to predict and optimize as new manufacturing materials and processes combine with the exploding number of features on a single IC. Though "Design-Existence" (first functional implementation) and "Design-Quality" (optimal implementation) may be separately defined, distinctions between the two blur when feature failure rates in the low ppb range can now result in zero yield. What may have been previously considered as a "quality" issue is often now an "existence" issue.

Clearly, new ways are needed to bring effective Design for Manufacturing (DFM) to the early stages of the Design cycle. Effective DFM technology must be able to predict quantitative yield, and now must incorporate statistical analyses of complex Process-Design interactions, instead of just design area modeling. Failures-per-feature must be resolved in the low ppb range, and Characterization Vehicle™ test chip technology is needed to calibrate such feature-based yield models for current manufacturing processes.

A calibrated feature-based model simulates the manufacturing yield due to Design and/or Process changes, allowing for "virtual spins" without the expenses of masks and silicon wafers. Design-Based Yield Improvement™ solutions can use virtual spins to substantially optimize Designs; this work must begin early in the Design phase to ensure that Design-Existence includes the maximum amount of Design-Quality.

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Dennis Monticelli, Fellow at National Semiconductor, Inc.
Quality will matter as much or more in our deep sub-micron future as it has in the past. Despite the challenges of insuring the quality of nanometer scale devices, semiconductor makers will succeed in making large-scale integrations with very good device quality and reliability levels. This is a battle on familiar ground and within an environment that the maker can control. Testing such devices will likewise be challenging, but with designers gradually accepting the concept of BIST, this hurdle will be surmounted as well.

The bigger issue is that of insuring complex SOCs enabled by nano-scaling will operate in the system in the manner intended. This broader definition of quality is not entirely within the control of the semiconductor vendor. As much as the system designer wants accountability here, success will not come often enough with conventional arm's length approaches. Standard products simply cannot contemplate every application. Even the highly detailed specifications prevalent in custom chip programs often have holes, resulting in unpleasant surprises when the system first comes together. At the high price of nano-scale tooling, not to mention time-to-market penalties, such surprises are ugly indeed. System makers must be willing to take component designers up the system learning curve and include them as a partner in the design process at as an early a stage as possible. Early involvement also insures optimal partitioning among chips and between hardware and software. The only other alternative for system designers is to sacrifice differentiation for the reduced risk of a "pre-cooked" reference design complete with software and BOM.

Resve Saleh, NSERC/PMC Sierra Chair Professor, UBC Vancouver
As a researcher in the field of UDSM SOCs, we address all of the dynamics in the application space for creating products. The large number of technical issues at all levels of design makes this a very complex issue to assign quality metrics to. The issue of Existence on a schedule for SOC designs has always been highest priority for the designer.

In order to address this goal, the key quality metrics have rightly been pushed to the component (IP) providers, fabs and most importantly the compliance of the IP and the fab with the design flows and tools being used. Device level design and understanding of the manufacturing process are the keys to SOC reliability and the expertise level to address these issues are outside of the experience base of most SOC designers.

In order to get first time working designs, the SOC designers need to use IP that are designed correctly, optimally configured for yield on the application and properly characterized to be used with the tools flows chosen. These are assumptions for the SOC environment and the scope of work for creating a 10M+ gate SOC does not allow for the support of those tasks.

Norm Towson, President and COU, Netcell Corp.
As an ASIC/SOC customer we do not have the luxury of being able to separate the two goals of Existence and Quality. Market place and funding pressures require us to create very aggressive design content on a short schedule AND have it work first time and in manufacturing.

Our focus is on the SOC architecture, functionality and software required to meet our application. The assumption is ALL IP we are using as well as ALL manufacturing processes are stable and will perform optimally as specified. Our schedules do NOT allow us to "re-validate" these assumptions that the cells are good, the tools work, or the fab can make the design - we can only accept them as fact. This is a position we have been forced into by the financial community which is driving the schedules.

We feel that for the UDSM technology SOC marketplace, the responsibility of quality of all materials in the supply chain resides with the providers of - cells and fab. This way, the end application user can rightfully deal with ONLY its application design and software.

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