
Tutorial D3

1:30pm – 3:00pm

NBTI/HCI Modeling and Full-Chip Analysis in Design Environment

Organizer: Lifeng Wu, Celestry

Presenter: Lifeng Wu, Celestry

Hot-carrier (HC) degradation and negative bias temperature instability (NBTI) of MOS devices are the two most important reliability concerns for deep submicron (DSM) designs. HC degradation occurs when the channel electrons are accelerated in the high electric field near the drain of the MOS device and create interface states, electron traps, or hole traps in the gate oxide near the drain. LDD structure has become the standard drain structure to alleviate HC effects and the device-based DC criteria have been used extensively to qualify devices for HC reliability. It is becoming clear that these guidelines are too conservative for DSM technologies. It is therefore strongly desirable that circuit reliability simulation using a realistic AC (transient) circuit operation condition should be on the fingertips of the circuit designers to achieve the following goals: to maximize design performance by minimizing design guard-band, to speed up timing closure by reducing design iterations and to ensure circuit reliability by fixing design reliability problems. How to fit reliability simulation into the design environment is a more interesting topic from designer's perspective.

Compared to the more matured studies and solutions on HC effects, the studies on NBTI reliability has just started. NBTI reliability is becoming an increasingly important as the thickness of gate oxide film scaled down to less than 50 Angstrom, which is common for DSM designs. Unlike HC degradation which needs high electric field at the drain, NBTI effect can be significant even when the drain-source is zero biased. This implies that circuits could undergo NBTI stress even at standby operation condition! NBTI effect becomes more severe under high temperature stress. The popular burn-in procedure is being re-considered by designers to maintain acceptable yield. The recovery of NBTI effect is another important issue to reduce design margin.

This tutorial provides an overview of the HC and NBTI effects including physics, impact on circuit performance, modeling and simulation technologies. Both full-chip transistor-level and gate-level solutions will be presented with million-transistor/gate capacity and high accuracy.