# **Tutorial Track D:** Design for Reliability

Chair and moderator: Mohsen Alavi, Intel Corporation

## Tutorial D1

***9:00am – 10:30am***

### Overview of Reliability Issues in Deep Sub-Micron Digital CMOS Technology and Their Interaction with Circuit Design Considerations

*Organizer:* *Mohsen Alavi, Intel Corporation*
*Presenter:* *Mohsen Alavi, Intel Corporation*

During the operation of integrated circuits, electrical and thermal stress result in wear out of circuit components and degradation of key parameters and ultimately, catastrophic failure. Often times, failure of product functionality in meeting desired operating specifications occurs due to these parametric shifts and long before catastrophic failure. Therefore, circuits designed to allow larger shifts in parametric degradation result in enhanced product reliability. Such design practice requires good understanding of physical mechanisms resulting in degradation and good models to predict it's behavior vs. stress. Furthermore, understanding of the statistics of degradation is needed to evaluate overall product failure rates.

As technology scaling reduces device dimensions and increases circuit complexity, the challenge of ensuring product reliability increases in two ways. Namely, many degradation mechanisms such as electromigration or soft error become more pronounced while tools and techniques to model degradation in more complex circuits become more challenging. Moreover, the continuous pursuit of circuit performance often results in a trade off with reliability such as the case with higher Vcc for faster products vs. dielectric reliability.

This tutorial presents an overview of various physical mechanisms resulting in device degradation and their relation to stress conditions in MOS logic technology. For each degradation mechanism, circuit impact and design consequences will also be discussed. Mechanisms will include hot carrier effects, transistor bias-temperature stability, gate dielectric wear out, plasma induced gate charging, interconnect electromigration, electro-static discharge (ESD), and soft error. Future challenges posed by technology scaling will also be discussed.

## Tutorial D2

***10:45am – 12:15pm***

### Noise Analysis for 0.13um and Beyond

*Organizer:* *Ken Tseng, Cadence Design Systems*
*Presenters:* *Kishore Singhal, Agere Systems*
*Vinod (Narayanan) Kariat, Cadence Design Systems*
*Ken Tseng, Cadence Design Systems*

At 0.13um and beyond, ignoring signal integrity is a luxury no designer can afford; SI issues are no longer the purview of high-performance designs. Hence most designers need an awareness of Signal Integrity analysis, prevention and correction. The presenters will draw on their experiences in Signal Integrity over the last several years to present a pragmatic and practical tutorial on noise analysis, prevention and correction.

Section 1: Fundamental Principles
In this section, we will discuss the fundamental issues that give rise to noise in digital designs. This will start with the technology trends that are giving rise to an increase in noise problems. Then we cover different types of noise effects and the factors that govern them. We will also discuss the fundamental principles of noise analysis.

Section 2: Noise Analysis, Prevention and Correction
In this section, we will discuss how noise effects influence different stages of the design flow, from early prototyping to final layout, including prevention and correction techniques.

Section 3: Experience with Noise Issues in the Design Flow
In this section, we will discuss several practical considerations associated with putting noise analysis techniques into the design flow. We discuss the approaches that yield reasonable results in practice.

Section 4: Future Considerations
This section covers some of the emerging issues that we expect to surface in the future due to technological and manufacturing considerations. We will cover issues associated with inductance, SOI, copper interconnect and various manufacturing rules.

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