Tutorial C2

10:45am – 12:15pm

An IC Design Perspective, “Why Would We Choose Flip Chip?

Presenter: *Scott Wood, STMicroelectronics*

1. Design requirements that drive to flip-chip
   a. Large numbers of IO
   b. Large numbers of power/ground connections
   c. High performance packaging
   d. High power consumption
   e. Nominal die size
   f. Multiple power supplies

2. Tradeoffs in flip-chip
   a. Peripheral bumps vs. full array
   b. Peripheral IO vs. core array IO

3. CAD problems to be solved
   a. IO design
   b. IO placement
   c. Single/multiple power grids
   d. Place and route
   e. Connectivity checking
   f. Co-design of PCB, substrate and silicon

Tutorial C3

1:30pm – 3:00pm

An EDA Perspective, “We Need it Yesterday!

Presenter: *Anna Fontanelli, STMicroelectronics*

1. Today’s design flows and their limitations
   a. Package driven or top-down
   b. IC driven or bottom-up

2. Co-design & co-verification
   a. Can do vs. worth doing, technology vs. economy
   b. Overlapping requirements
   c. IO and bumps placement
   d. Reliability
   e. Flip-chip
   f. Electrical & physical verification

3. Tools, methodologies and skills
   a. Current status @ ST
   b. Commercial vs. proprietary tools
   c. Interoperability issues
   d. Examples

Tutorial C4

3:15pm – 4:45pm

An EDA Perspective, “Let’s do it Concurrently!

Presenter: *Kevin Rinebold, Synopsys*

1. The silicon-package relationship
   a. Customers requests and industry responses
   b. Goals and challenges

2 Co-design
   a. Feasibility and trade-off analysis
   b. Concurrent IC & package design planning
   c. New tools and methodologies
   d. Examples

3 Co-verification
   a. Parasitic extraction and electrical modelling
   b. Full-chip characterization
   c. New tools and methodologies
   d. Examples

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