Tutorial Track C: IC and Package Co-Design

Chair and moderator: Marco Casale-Rossi, STMicroelectronics

Enhancing the Silicon-Package Interface Through Their Concurrent Design and Verification

Organizer: *Marco Casale-Rossi, STMicroelectronics*
Presenters: *Rich Evans, STMicroelectronics*
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Driven by nanometer silicon process and system-on-chip (SOC) technologies, the complexity of today's integrated circuits (IC) combined with their high pin-count and performance requirements has resulted in a more complex silicon-package interface than seen with traditional devices.

To address these challenges companies are increasingly choosing ball-grid array (BGA) substrates and flip-chip as their preferred IC to package interconnect mechanism. While BGA offers a great deal of opportunities in terms of package customization, flip-chip addresses the high pin-count requirement and provides the benefit of reduced parasitics.

Unfortunately most design methodologies result in a segregated relationship between IC and package, making coordinated planning a difficult and time-consuming task. The serial nature of the traditional silicon to package design flow limits the effectiveness of existing tools for concurrent planning. Both IC and package design tools lack the needed visibility into their respective neighboring environments to be of use. This serial approach may lead to a poor IC to package netlist resulting in overly complex custom package designs, increased packaging costs, longer cycle times and less than optimal silicon performance. Although BGA and flip-chip provide a vehicle to interface high performance silicon to the system, a methodology change is needed to realize its full performance potential.

This tutorial will give an overview about BGA substrates—pointing-out the strengths and the limitations of flip-chip vs. wire-bonding—, introduce the reasons and methods for co-design, and explore a new methodology that incorporates packaging as part of the silicon floor planning phase. New tools will be presented that facilitate coordinating planning and sharing of data across the two domains of silicon and package. The tutorial will show how coordinated planning during the early stages of IC floor planning will result in an optimized silicon/package interface, ultimately lowering cost, reducing cycle-time and enhancing overall device performance.

Tutorial C1

9:00am – 10:30am

A Package Design Perspective, "It will be BGA and Flip-Chip

Presenter: *Rich Evans, STMicroelectronics*

1. BGA design flexibility
   a. BGA basics and configurations
   b. Pin-out and footprint
   c. Wire-bonding: signals, power, ground
   d. Flip-chip configurations

2. Discussion of the basic limitations of flip-chip
   a. Dimensions
   b. I/O count
   c. Limitations on design – bump size, pitch, reliability, substrate capability
   d. Examples

3. Reasons and methods for co-design
   a. Considerations for high I/O count, high performance design
   b. Reasons for flip-chip and for co-design
   c. Design variables
   d. System, IC, package requirements
   e. Examples of packages where co-design was applied
   f. Specific flip-chip design issues

4. Flip-chip electrical performance
   a. Inductance
   b. High-speed serial links
   c. Power distribution

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