
Tutorial B3

1:30pm – 3:00pm

Design Based Yield Improvements (DBYI)

Organizer: Enrico Malavasi, PDF Solutions, Inc.

*Presenters: Enrico Malavasi, PDF Solutions, Inc.
Stefano Tonello, PDF Solutions, Inc.*

The manufacturability of integrated circuits can be improved at design level by incorporating modifications in the structure of the IP components (cores, cells, memories) and of interconnections, as well as changes in the design methodology and flow. In this tutorial we will describe the types of design improvements that can be introduced in the design of large integrated circuits, and the potential advantages they can have for yield. These include modifications in IP cores, standard cell libraries and memory blocks, as well as interconnections. The potential impact of different techniques on the design flow will also be discussed. We will describe the technology we use to quantitatively estimate and measure yield losses due to random, systematic and parametric effects. This capability is essential to drive design modifications, in order to understand their impact, and the trade-off between conflicting requirements.

Tutorial B4

3:15pm – 4:45pm

Yield in flash memory: Methodology, modeling and design issues

Organizer: Giuseppe Crisenza, STMicroelectronics

Presenter: Giuseppe Crisenza, STMicroelectronics

In the manufacturing of Flash Memory the main defective layers are metals, vias, polysilicon and contacts. Inside a Flash Memory, most of the area is utilized for memory array with around the decoding and multiplexing circuitry. In these regions, all buses in metal and polysilicon layers are designed with the minimum layout rules admitted by technology, to match the pitch dimension of the flash cells. As the number of steps, the number of cells, and the circuit density increases, and the critical defect sizes decreases, an increasing number of defects are only seen as electrical faults. Starting from the electrical signature to the physical defect identification, a collection of various defects, typical of Flash NOR array was identified and associated with methods for electrical screening. A yield model for Flash Memories with redundancy will show the effect of the three principal factors (systematic, defect and out layer related) allowing a faster analysis of yield limiting conditions. The decomposition of yield in the described factors allows the individuation of fields where the corrective actions have to be performed and the related strategies. For defectivity yield enhancement the corrective actions are the reduction of particles or point defects: in some case a simulation methodology is proposed in order to confirming the electrical signature. For systematic yield enhancement, robustness of the circuital blocks both layout and design, and of the testing flow are the principal issues addressed.