

# Tutorial Track B: Design for Manufacturing and Yield

Chair and Moderator: Duane Boning, Massachusetts Institute of Technology

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## Tutorial B1

9:00am – 10:30am

### Testing and Yield of Integrated Circuits

*Organizer:* Zoran Stamenkovic, IHP GmbH

*Presenter:* Zoran Stamenkovic, IHP GmbH

Yield is one of the cornerstones of a successful integrated circuit (IC) manufacturing technology along with product performance and cost. Many factors contribute to the achievement of high yield but also interact with product performance and cost. A fundamental understanding of yield limitations enables the up-front achievement of this technology goal through circuit and layout design, device design, materials choices and process optimization. Defect, failure and yield analyses are critical issues for the improvement of IC yield. In the first part, we deal with IC fault models and test issues. The second part describes critical area models and yield models. The third part is dedicated to a local extraction approach for the extraction of IC critical areas. Finally, we present an application of above-mentioned models and extraction approach in yield forecast.

## Tutorial B2

10:45am – 12:15pm

### Test Structures for Circuit Yield Assessment and Modeling

*Organizer:* Prof. Duane Boning, MIT

*Presenters:* Prof. Duane Boning, MIT

Prof. Anthony Walton, University of Edinburgh

Dr. Christopher Hess, PDF Solutions

The assessment and modeling of process variation and defectivity is becoming increasingly important in the design of high-yielding and high-performance integrated circuits. Process variation is coming from a number of sources: in addition to lot and wafer level variation, within chip variation arising from pattern dependencies is of substantial concern, affecting the matching of device and interconnect parameters. The understanding of defect sources and their impact and interaction with the layout continues to be critical to achieving required yields.

The focus of this tutorial session is on test structure methodologies for yield assessment and modeling. The first segment will describe a circuit-level test structure approach, which enables the extraction and characterization of layout practice and pattern dependent effects on delay in circuits. A scan-chain approach is coupled with a large number of ring oscillator variants, so that the impact of process and layout variations on realistic circuit timing can be extracted.

The second segment will describe test structures for measuring parametric characteristics such as linewidth, resistivity, contact resistance, layer thickness, etc., as well as standard transistor parameters at the device level. Wafer mapping variations of these parameters with a view to identifying root causes will be briefly discussed. The section will conclude with the presentation of methods for increasing the number of devices on testchips through the use of active on-chip switching.

Finally, the third segment will describe “Universal Characterization Vehicles” that combine a variety of test structures on a single chip. It covers systematic and random yield characterization like defect densities, defect size distributions and fail rates, which are important input for DFM. It also includes structures that drive SPICE modeling including statistical SPICE models for advanced analog designs. Such vehicles can evaluate the entire process flow or just a fraction of it as a short loop to decrease cycle time. This segment will cover methods for advanced area usage as well as improved test procedures that significantly reduce test time.