

Tutorial Track A: Design for Yield Optimization and Test

Chair and Moderator: Yervant Zorian, LogicVision

This tutorial is part of the IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2003

Tutorial A1

9:00am – 12:15pm

Integrating Yield, Test and Reliability: “Statistical Models with Applications to Test and Burn-in Optimization”

Organizer: Adit Singh, Auburn University

Presenter: Adit Singh, Auburn University

Recent research has shown that die yield, test effectiveness, and early life reliability of integrated circuits are closely interrelated because of the common underlying statistics governing the distribution defects on semiconductor wafers. An understanding of these relationships can allow test effort, including burn-in screening, to be weighted in favor of sub population of dies with the highest expected failure rates. Consequently, the lowest possible defect levels (DPM) and field failure rates can be achieved at minimum overall test costs. This tutorial will introduce statistical yield-reliability models and show how they can be used for test optimization.

Tutorial A2

1:30pm – 4:45pm

Optimizing the Yield of VLSI Circuits

Organizer: Israel Koren, University of Massachusetts

Presenters: Julie Segal, HPL Technologies

Israel Koren, University of Massachusetts

Yield optimization effort must involve all area of semiconductor engineering: design, manufacturing, and test. This tutorial presents an overview of techniques for projecting and optimizing the yield of VLSI circuits, including high density memories, microprocessors and other architectures. Many of these techniques are being currently used in manufactured integrated circuits and will be reviewed. The nature of manufacturing defects is discussed in this tutorial, and the need for incorporating defect tolerance and/or yield enhancement techniques in the design of complex VLSI chips is explained. Then, some commonly used models for yield projection are presented. These models serve to evaluate the effectiveness of the proposed techniques and to calculate the optimal amount of circuit modifications.