

# RC Power Bus Maximum Voltage Drop in Digital VLSI Circuits

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## Abstract

*This paper presents an input-independent method for finding bounds on the voltage drop in RC power bus in digital VLSI circuits. The voltage at power bus nodes is expressed in term of gate currents using sensitivity analysis. Circuit timing information, functionality and logic dependencies are employed to find maximum simultaneous HL and LH switching in a clock subinterval. The sensitivity information together with an optimization procedure are applied to find bounds on the voltage drop in targeted bus nodes.*

## 1 Introduction

The current requirements in the modern VLSI designs elevate as the level of circuit integration increases. Consequently, power delivery has become a critical issue in VLSI designs. The situation is further complicated due to the parasitics in the power distribution networks as well as the time-varying nature of the demand of the current. It is widely known that lower voltage supply increases pin-to-pin delays. Therefore, voltage variations in power distribution networks often have negative impacts on the performance and reliability of the circuits. The timing margins are becoming extremely limited as the clock frequency increases. Hence, it is desirable to model as many uncertainties as possible during the design process. Techniques that can accurately estimate the worst-case voltage variations are required. This is the focus of the paper. The worst-case IR voltage drop at nodes in the power bus can be obtained using VMAX [2]. Although a resistive model for the power distribution network to compute IR drop simplifies the analysis, it completely ignores any decoupling capacitance that helps to reduce the voltage drops.

In this paper, we present a new input-independent approach to compute tight upper bounds on voltage drops in the RC power distribution network. We first apply frequency domain sensitivity analysis to obtain the sensitivity vector. Then it is transformed back to the time domain. The voltage variations at the bus nodes can be expressed as the summation of convolutions of gate currents and time varying sensitivity vectors. Based on static timing analysis, the gate current waveforms are constructed within their uncertainty switching intervals [2, 3]. Bound on maximum voltage drop at a node during a time sub-interval is formulated as an optimization problem that takes into account the functional dependencies in the design. The solution of the optimization problem gives the upper bound on the voltage drop in that sub-interval. When there are large decoupling capacitances connected to the power bus, the voltage drop at the nodes in the power bus may not restore to zero at the end

of clock cycle. This means that the worst-case voltage drop at the nodes may increase in the next clock cycle. In this case, finding the steady-state solution will be necessary. This can be achieved by applying periodic maximum gate current envelopes as will be explained in the sequel.

## 2 Maximum Voltage Drop in RC Power Bus Models

In [2], the authors presented a approach to compute the worst-case maximum voltage drop in the resistive power bus. For RC power bus network, steady-state is not reached instantaneously as in the purely resistive model. For this reason, the method of estimating bounds on the voltage drop as describe in [2] can't be applied directly. Applying Laplace transform to the bus circuit equations with zero initial conditions, we get:

$$(\mathbf{G} + \mathbf{sC})\mathbf{V}(\mathbf{s}) = \mathbf{I}(\mathbf{s}) \quad (1)$$

$\mathbf{G} + \mathbf{sC}$  is admittance matrix.  $\mathbf{I}(\mathbf{s})$  is the Laplace transform of the current waveform drawn by the gates. The frequency spectrum of the maximum voltage drop waveform at node  $j$  is:

$$V_j(\mathbf{s}) = \mathbf{e}_j^T \mathbf{V}(\mathbf{s}) \quad (2)$$

Using Eq. (1), it is easy to derive:

$$V_j(\mathbf{s}) = \mathbf{e}_j^T (\mathbf{G} + \mathbf{sC})^{-1} \mathbf{I}(\mathbf{s}) \quad (3)$$

If we define:  $\mathbf{e}_j^T (\mathbf{G} + \mathbf{sC})^{-1} = \mathbf{\Psi}_j^T$  (4) where  $\mathbf{\Psi}_j$  is the frequency domain sensitivity vector of node  $j$ . The frequency spectrum of  $V_j(\mathbf{s})$  equals to the inner product of vectors  $\mathbf{\Psi}_j$  and  $\mathbf{I}(\mathbf{s})$ . In time domain,  $v_j(t)$  can be expressed as summation of the convolution between corresponding elements from these two vectors. The sensitivity vector  $\mathbf{\Psi}_j(\mathbf{s})$  can be calculated by solving Eq. (5).

$$(\mathbf{G} + \mathbf{sC})\mathbf{\Psi}_j(\mathbf{s}) = \mathbf{e}_j \quad (5)$$

The sensitivity vector  $\mathbf{\Psi}_j$  is frequency dependent. Eq. (5) needs to be solved at different frequencies. Let  $T_{clk}$  be the user specified clock period.  $T_s$  is the sampling time. The  $N_s$  frequency domain samples are selected from  $-F_s/2$  to  $F_s/2$  with step  $F_s/N_s$ , where  $F_s = 1/T_s$  and  $N_s = T_{clk}/T_s$ . After all the samples of the sensitivity vector in the frequency domain are found, they are transformed back to time domain. The voltage drop waveform  $v_j$  can be expressed as the convolution of vector  $\mathbf{\Psi}_j^T$  and  $\mathbf{I}$  in time domain.

$$v_j(t) = \int_0^{T_{clk}} \sum_{i=1}^{g_N} \Psi_{ij}(\tau) I_i(t - \tau) d\tau \quad (6)$$

$g_N$  is the total number of gates in the circuit. Each element of the time domain sensitivity vector is a time dependent variable. We have  $N_s$  samples for each of this variable distributed evenly from 0 to  $T_{clk}$ . The current envelope drawn

by each gate is also sampled at the same time instants. Because  $\Psi_{ij}(t)$  and  $I_i(t)$  are sampled at discrete time instants, the integration in Eq. (6) becomes a summation as shown in Eq. (7).

$$v_j(nT_s) = \frac{T_{clk}}{N_s} \sum_{i=1}^{g_N} \sum_{k=0}^{N_s-1} \Psi_{ij}(kT_s) I_i[(n-k)T_s] \quad (7)$$

In Eq. (7), the maximum voltage drop at node  $j$  at time  $nT_s$  is expressed as the summation of contributions from all the switching gates. The contribution from each gate is applied as the weight of a vertex in the constraint graph [2]. Constraint graph optimization [2] is then applied to find an independent set of gates that cause the worst-case voltage drop of  $v_j$  at time instant  $nT_s$ .

If all the node voltages drop are not restored to zero within the clock period, then simulation of the RC power bus for a number of cycles would be required to estimate the worst-case voltage drop. This problem is precisely the problem of finding the steady-state response of a linear circuit with a periodic input excitation. The steady-state solution can be achieved by using periodical maximum current envelopes as inputs. The voltage drops are guaranteed to be steady-state solution. Circular convolution is required in the computation. Following is the only modification in Eq. (7) when  $n - k < 0$ ,

$$I_i[(n - k)T_s] = I_i[(n - k + N_s)T_s] \quad (8)$$

The following four techniques are proposed to reduce computation time. First technique is parallel programming. Parallel programming is applicable in this case because the procedures for finding worst-case voltage drop waveforms at different nodes in the power bus are independent of each other. The second technique reduces the number of nodes that have to be analyzed by classifying a violation node in the power as the node connected to logic gate and have larger voltage drop than a user specified threshold value. In order to identify the violation nodes, we apply *iMax* [3] first. Thirdly, the number of violation nodes of interest at any given time point can be further reduced by focusing only on the nodes connected to switching gates at any given time point since they are the gates whose performance are affected by the voltage drop across them. Fourth, the size of the constraint graph can be reduced in order to speed up the simulation. This is achieved by finding the vertices that have weights below a certain threshold and eliminating them from the constraint graph. At every time point, the vertices are sorted according to their weights, with the vertex having the highest weight selected first. Vertices are then selected based on their weights in descending order until the summation in Eq. (7) reaches a certain percentage of the total sum. The simulation speed can increase 12 by using this technique.

### 3 Simulation Results

As a first example, we compare our results with HSPICE exhaustive simulation results using a simple combinational circuit with three primary inputs. The clock period is chosen long enough so that the voltage drops of all the nodes in the power bus are restored to zero at the end of clock cycle. Fig. 1(a) shows the comparison of our simulator and HSPICE exhaustive simulation results. There is a maximum of 55% over-estimation between VMAX and HSPICE. One of the reason for this over-estimation could be the following. Signal statistical variations are not considered during HSPICE exhaustive simulation. But in a real integrated circuit, due to process variations and cross-coupling capacitance effects, the

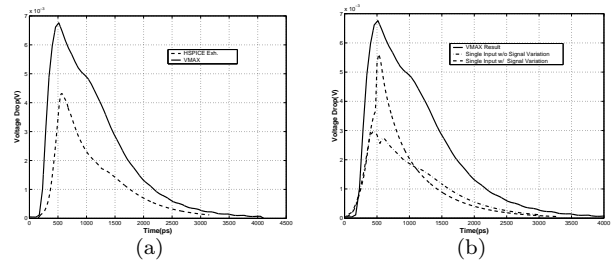


Figure 1: VMAX and HSPICE exhaustive simulation comparison and the signal statistical variations effects

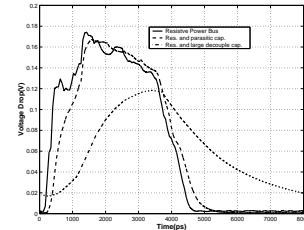


Figure 2: Worst-case voltage drop using different model

delay of standard cell is not constant. The signal switching time instant should also be statistically distributed within a certain range. The worst-case voltage drop will also be affected by this statistical variation. Our approach can implicitly include the statistical variations of gate currents and timing. Fig. 1(b) shows the worst-case voltage drop waveform at the target node caused by the single input vector with and without signal statistical effects. The maximum instantaneous voltage drop value increases by 33.3% after considering signal statistical variations.

Fig.2 shows the worst-case voltage drop at a node in benchmark circuit C1355 power bus. There are three curves in the figure, one is derived using resistive power bus model. The second uses an RC model. For the third curve, we assume there are some large decoupling capacitances attached to the power bus. Obviously, when there are large decoupling capacitance attached to the power bus, the voltage drop does not go to zero at the end of the clock period, and steady-state analysis becomes necessary.

### 4 Conclusion

In this paper, we presented a frequency domain sensitivity analysis-based algorithm for estimating the maximum voltage drop in RC power bus in a digital VLSI circuit. The simulator can estimate the worst-case voltage in a fast and accurate way. Signal statistical variation effects on the maximum voltage drop are automatically included. Several techniques are also introduced to speed up the simulation.

### References

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