# Test Pattern Generators for Distributed and Embedded Built-In Self-Test at Register Transfer Level

Vladimir Vorisek
*Institute of Informatics, Slovak Academy of Sciences*
*vorisek.ui@savba.sk*

## Abstract

*The poster presents Ph.D. thesis in the area of Test Pattern Generators (TPGs) for application in distributed and embedded Built-In Self-Test (BIST). The goal of this work is to develop a general scheme of designing built-in TPGs for basic arithmetic elements such as adders, subtracters, multiplexers, comparators at Register Transfer Level (RTL) of circuit description.*

## 1. Introduction

Off-line structural Built-In Self-Test (BIST) techniques are well known for testing complex digital VLSI circuits and a lot of papers were published in this area. Verifying structural integrity of circuits, rather than their functional performance, is becoming more popular.

This work deals with so-called distributed and embedded BIST that consists of many Test Pattern Generators (TPG) and Test Response Analyzers (TRA) distributed along Circuit Under Test (CUT), i.e. every functional block has its own dedicated TPG and TRA, and these TPGs and TRAs are embedded into the functional blocks of CUT. The goal of this thesis is to develop a library of TPGs dedicated to the basic RTL elements such

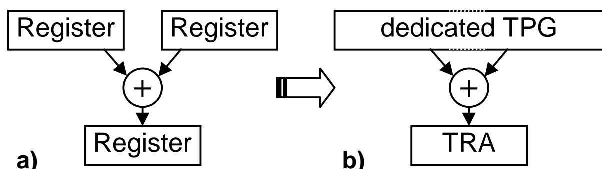


**Figure 1. Example of distributed and embedded BIST**

as adders, subtracters, multiplexers, comparators for BIST where TPGs and TRAs are distributed along these basic RTL elements and build up with functional registers of CUT. In normal functional mode of CUT every register takes its own function (Figure1a) and in test mode these registers are reconfigured into special TPGs and TRAs dedicated to surrounded RTL element (Figure 1b). This concept allows at speed testing, reduces area overhead and with efficient TPGs provides very high fault coverage. Since such BIST circuitry is implemented at the RTL level of description, test synthesis will run much faster and get more reasonable results than the gate level BIST, which will improve the overall quality of the design.

## 2. Technical Background

Pseudo-Random Pattern Generators (PRPG) are commonly used in function of TPGs. They produce so-called pseudo-random patterns, which are not truly random but have properties of random patterns. PRPGs are commonly realized by finite state machines, such as the Linear Feedback Shift Register (LFSR) or the Hybrid Linear Cellular Automata (CA).

The evolution of finite state machines can be best exemplified by means of the time-state diagrams. In this technique, each cell of a circuit has a vertical black pixel assigned if the corresponding bit is a logical one. In Figure 2, beginnings of time-state diagrams of common PRPG examples are shown.

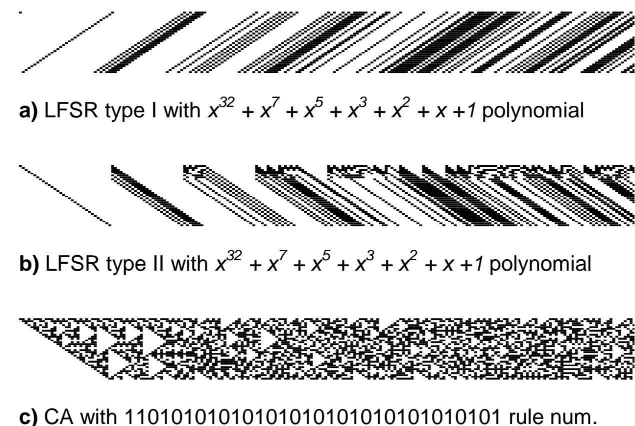


**Figure 2. Time-state diagrams of common PRPG**

Proceedings of the International Symposium on Quality Electronic Design (ISQED'01)
0-7695-1025-6/01 $10.00 © 2001 IEEE

However, such PPRGs can not guarantee complete fault coverage if the CUT contains Random Pattern Resistant faults (RPR faults). Various techniques have been introduced (weighted random patterns, pseudo-exhaustive patterns and deterministic patterns) to improve RPR faults coverage. But these techniques cause additional disadvantages as implementation difficulties and high hardware overhead.

The objective of this Ph.D. theses is to develop built-in TPGs for basic RTL elements with the goal to find the most efficient pattern generators with high fault coverage and a small number of run cycles.

**Table 1. Testability simulation of basic RTL elements**

| RTL element | | | Random | | LFSR type I | | LFSR type II | | CA | |
|---|---|---|---|---|---|---|---|---|---|---|
| Arith. | width | faults | cycle | cover | cycle | cover | cycle | cover | cycle | cover |
| **Bus** | 32 | 64 | 6 | 100 | 32 | 100 | 32 | 100 | 32 | 100 |
| **Reg** | 32 | 256 | 32 | 100 | 60 | 100 | 60 | 100 | 66 | 100 |
| **Mux** | 32 | 450 | 32 | 100 | 128 | 100 | 126 | 100 | 128 | 100 |
| + | 32 | 1000 | 64 | 100 | 64*<br>661 | 72,40<br>100 | 64*<br>725 | 72,40<br>100 | 118 | 100 |
| – | 32 | 1128 | 64 | 100 | 64*<br>698 | 97,25<br>100 | 64*<br>575 | 97,25<br>100 | 112 | 100 |
| × | 32 | 32 127 | 1 024 | 100 | 1 584 | 100 | 1 646 | 100 | 293 | 100 |
| ÷ | 32 | 34 026 | 1 024 | 77,05 | 692 | 99,59 | 351 | 99,28 | 10k | 82,14 |
| > | 4 | 108 | 192 | 100 | 100 | 100 | 158 | 100 | 152 | 100 |
| | 8 | 220 | 2 272 | 100 | 17*<br>3 310 | 90<br>100 | 16*<br>1478 | 87,73<br>100 | 886 | 100 |
| | 16 | 444 | 100k | 98,2 | 33*<br>100k | 90,09<br>99,77 | 32*<br>1 273 | 88,51<br>97,07 | 100k | 95,95 |
| | 32 | 892 | 100k | 53,14 | 64*<br>2 082 | 89,35<br>97,53 | 64*<br>100k | 88.90<br>95,52 | 100k | 55,27 |
| = | 4 | 52 | 64 | 100 | 47 | 100 | 37 | 100 | 72 | 100 |
| | 8 | 112 | 1 504 | 100 | 12*<br>2 840 | 64,29<br>100 | 16*<br>49 | 78,57<br>100 | 887 | 100 |
| | 16 | 216 | 100k | 84,26 | 26*<br>33 725 | 68,52<br>100 | 32*<br>257 | 79,63<br>100 | 100k | 95,37 |
| | 32 | 428 | 100k | 1,4 | 61 | 77,10 | 64* | 79.91 | 100k | 3,27 |

* stands for walking 1 sequence

## 3. Testability Analyses and TPG "fitting"

Most approaches to the synthesis of built-in self test circuitry use a manual choose-and evaluate approach, where a particular BIST generator is chosen and then evaluated by fault simulating with the vectors that the chosen generator produces.

In this work basic RTL elements have been fault-simulated with randomly generated patterns and with three different types of pseudo-random patterns (LFSR type I, LFSR type II and CA). Simulated results (Table 1) show, which type of PRPG (shaded areas of Table 1) can be efficiently used for a certain RTL element. It also shows that for some types of elements the walking 1 sequence (generated at the beginning) covers quite high percentage of faults.

As it can be seen from Table 1, busses, registers, and multiplexers are highly random pattern testable, but comparators are highly random pattern resistant.

## 4. Conclusion

The main contribution of this Ph.D. thesis is aimed at the construction of efficient TPGs for distributed and embedded BIST at the register transfer level. It was shown which types of PRPGs are most efficient to use to generate test patterns for certain RTL elements. Future work of this thesis will be to develop a special RTL library of TPGs dedicated to RTL elements which are random pattern resistant.

## 5. References

[Gho00] I. Ghosh, N. K. Jha, "A BIST Scheme for RTL Circuits based on Symbolic Testability Analysis", in *IEEE Transactions on Computer aided Design of Integrated Circuits and Systems,* vol. 19, no. 1, January 2000, pp. 111-128.


0-7695-1025-6/01 $10.00 © 2001 **IEEE**