

Refinements of Rent's Rule allowing Accurate Interconnect Complexity Modeling

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Abstract

The complexity of the interconnect topology of a circuit is well captured by Rent's rule. This rule can be applied for a priori wire-length estimation, which is useful for improving the quality of generated layouts, and could be used for reducing the number of design iterations. It can also successfully be applied for the generation of synthetic benchmark circuits. However, Rent's rule is an empirical approximation, and there are many deviations. This paper describes possible extensions to Rent's rule and discusses some of its applications.

1. Introduction

With the continuing evolution of VLSI technology, more and more gates are being pushed on a single chip. The design of chips becomes more complicated, and the problem is worsened by deep submicron effects due to the ever shrinking feature size. As die sizes keep growing, and clock periods keep shortening, the delay of global interconnections becomes more critical. Since most of the designs are interconnection dominated – most of the area of contemporary chips is occupied by wires, and this is also where most of the delay can be found – it is crucial to model the interconnection complexity as accurately as possible at each stage of the design cycle.

The interconnection complexity of a circuit is well captured by Rent's rule [2] and the corresponding Rent exponent. This rule has been applied numerous times, especially in the field of a priori wire-length estimation. A more recent application is the generation of realistic synthetic benchmark circuits.

However, Rent's rule is an empirical law that holds on average, and many deviations exist. This has been the cause

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for quite a few misinterpretations. The goal of this research is to analyze the strength and limitations of Rent's rule for the purpose of computer-aided design of VLSI circuits. In Section 2 we will describe the basics of Rent's rule and address a few possible extensions. Applications to Rent's rule will be discussed in Section 3. The paper ends with some concluding remarks in Section 4.

2. Rent's rule

Rent's rule states that, for different partitions of more or less equally sized modules of a circuit, obtained by a certain net cut minimizing method, there exists a power law relationship between the average terminal count T_{avg} and the average module size B_{avg} :

$$T_{avg} = kB_{avg}^p \quad (1)$$

Here, k is the *Rent coefficient* which corresponds to the average number of ports, and p is the *Rent exponent*. The validity of this rule is a result of the *self-similarity* that exists in real circuits. A high Rent exponent implies many global interconnections, and hence a high interconnection complexity. Generally, p ranges from 0.47 for regular circuits, such as RAMs, up to 0.75 for complex circuits, such as fast full custom VLSI circuits.

For large module sizes, which corresponds to the highest levels of the hierarchy, the number of terminals quite often appears to be lower than expected from (1). This deviation of the data from the main power law of Rent's rule is known as region II in Rent's rule. It can be intrinsic to the functionality of the circuit, but it is mostly due to technological constraints, such as pin-limitation of contemporary packages.

Some circuits also show a deviation from Rent's rule for low values of T and B , which can be referred to as region III. It occurs when a mismatch exists between the average number of block ports and the Rent coefficient k .

Rent's rule can be extended in various ways. The module terminals consist of inputs and outputs, and similar empirical relationships can be observed for the module inputs and outputs individually. These extensions prove to be very useful for synthetic benchmark generation, which will be discussed further.

Rent's rule describes first-order statistics of the terminal-count distribution for different partitions of the circuit. A simple stochastic model can be derived to describe higher-order statistics. Circuits that follow Rent's rule are considered homogeneous. At higher levels of the hierarchy mismatches may occur due to heterogeneity. This heterogeneity and the impact on the Rent characteristics can be modeled as well. Details on the stochastic properties of Rents rule can be found in [5].

3. Applications to Rent's rule

Wire-length estimation

A priori wire-length estimation is receiving more attention recently. It is being used in various models for layout parameter estimation. A good overview of different wire-length estimation models is presented in [1]. Such estimations could be extremely valuable for the interaction between logic synthesis and physical design. During synthesis, tight wire-length constraints can be set on the individual nets in accordance with the wire-length distribution, which allows accurate delay estimation. Because of the accurate estimation of the wire-length distribution, the wire-length constraints can be met during the physical design stage. This approach could guarantee timing closure with fewer – ideally zero – design iterations.

To the best of our knowledge, in all currently published research papers a homogeneous circuit model with deterministic Rent behavior has been applied. This is a very crude approximation, and corresponds to estimating the average of a function evaluated in a set of points by the function value of the average of those points. A stochastic derivation of the wire-length distribution allows a more correct estimation of the expected wire-length distribution.

The Rent parameters characterize both the circuit and the partitioning algorithm. Since partitionings induced by circuit placement have very variable Rent characteristics, it is almost impossible to get accurate estimations. Little variation in Rent exponents, and the existence of Region II limits the predictability of wire-lengths distributions.

Synthetic benchmark generation

Because Rent's rule expresses the fundamental properties of the circuit topology, it is also very suitable for the generation of realistic synthetic circuits. The development and

evaluation of new technologies, architectures and electronic design automation tools requires a substantial amount of benchmark circuits. Because of the proprietary nature of industrial circuits, it is almost impossible (for the research community) to compile benchmark suites from existing designs. Recently, synthetic benchmarks are being recognized as a viable alternative [6]. Furthermore, the use of synthetic benchmark suites has extra advantages, such as full control over the important characteristic parameters. Ideally, those parameters can be set independently, and one has full control over the granularity of the synthetic benchmark suites.

Our method is based on bottom up clustering according to Rent's rule. It offers perfect control over the interconnection complexity at different hierarchical levels. This method was augmented with a combinational loop prevention scheme [3]. Recently, it has been extended with controlled delay and stochastic properties of the generated circuit [4].

4. Conclusions and future work

Rent's rule is an empirical law that captures the interconnection complexity of a circuit. It can be applied for a priori wire-length estimation. Due to heterogeneity and the stochastic nature of self-similarity, the accuracy of these estimations is limited.

Rent's rule has been extended with directionality information, which results in expressions for the number of in- and outputs as function of the module size. It forms the ideal basis for a synthetic benchmark generation method based on bottom-up clustering.

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