

## Plenary Speech 2P.4

### Quality of SoC designs through quality of the design flow: Status and Needs

**Wednesday, March 28**

*11:10am-11:50am*



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It is now universally recognized that System-on-Chip (SoC) is the appropriate product solution to meet the demand of cost and volume for many electronics markets. The increasing pressures coming from shrinking market windows, accelerating process roadmaps and increasing mask costs, render necessary that SoC be correct at first silicon. This is becoming a considerable challenge due to the complexity of systems that can be built on the same chip: current process capabilities are approaching 100 million devices. Additionally, this level of integration comes at the price of renewed parasitic effects, such as crosstalk, voltage drop and electro-migration.

A complex design flow is necessary to solve these conflicting trends, combining executable specifications, isolating function from communication, exploring architectures and trading off speed, power, area and schedules, and finally a fast route to implementation, be it in software running on embedded processors, dedicated digital hardware, or dedicated analog cells. The successive levels of abstraction of the system description warrant the need for extensive verification of the SoC, both at functional level, and at the timing, power and reliability levels.

Building such a design flow calls for mixing very good point tools, coming from established EDA vendors as well as start-ups and academia. But above all, it requires well-defined and structured interfaces between tools at key hand-off points in the design flow. Standard design languages and Application Programming Interfaces (API's) are fundamental to the success of SoC.

#### **About Philippe Magarshack**

Philippe Magarshack graduated from Ecole Polytechnique and Ecole Nationale Supérieure des Télécommunications in Paris, France in 1985. He participated to the design of the 32-bit microprocessor family of AT&T Bell Labs from 1985 to 1989, in New Jersey, Pennsylvania and California. In 1989 he joined Thomson-CSF in Grenoble, France, and took responsibility for libraries and ASIC design kits for the military market. In 1994, he joined SGS-Thomson's Central R&D Group, where he now heads the central CAD and library activities, providing design solutions on CMOS and BICMOS platforms in 0,25um, 0.18um and now 0.12um technologies.