Plenary Speech 2P.1

Quality of Design from an IC Manufacturing Perspective

Wednesday, March 28
8:45am-9:25am

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There are many credible sources (including the ITRS) now seeing cost of IC manufacturing as a potentially negative factor that may affect the future of the IC industry. There are also a number of answers to the growing-cost-of-manufacturing challenge. One of them is IC design for efficient manufacturing — measured by such indices as yield, time-to-volume, etc.

The first objective of this presentation is to analyze publicly discussed visions for the IC industry and derive from them manufacturability conditions that must be met for these visions to materialize. We will focus our discussion on the recent version of the ITRS. It will be shown that ITRS predictions cannot be fulfilled by design or manufacturing approaches alone. Only by solving complex trade-offs on the design-test-manufacturing interface one may provide a chance to overcome the rising-cost-of-manufacturing problem — the main stumbling block on the
ITRS horizon.

The second objective of the presentation is to propose a redefinition of the notion of the quality of IC design, so it can accommodate manufacurability measures as primary design goals in addition to traditional die size, performance and time-to-first-silicon design quality indices. Such a re-definition is possible and maybe necessary contribution of the IC design community in addressing the rising-cost-of -manufacturing problem.

About Wojciech P. Maly

Wojciech Maly received the M.Sc. degree in electronic engineering from the Technical University of Warsaw, Poland, in 1970, and the Ph.D. degree from the Institute of Applied Cybernetics, Polish Academy of Sciences, Warsaw, Poland, in 1975. From 1970 to 1973, he was with the Institute of Applied Cybernetics. In 1973, he joined the Technical University of Warsaw, where he was appointed Assistant Professor in 1975. From September 1979 to July 1981, he was a Visiting Assistant Professor of Electrical and Computer Engineering at Carnegie Mellon University, Pittsburgh, PA. Since September 1983, he has been with Carnegie Mellon University, where he is a Whitaker Professor of Electrical and Computer Engineering. Dr. Maly's research interests have been focused on the interfaces between VLSI design, testing and ...

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manufacturing with the stress on the stochastic nature of phenomena relating these three VLSI domains. He has authored, co-authored and edited a number of books, journal and conferences papers, as well as patents, which have attempted to promote integration of design, test and manufacturing. Among his publications addressing the above field are papers introducing: statistical process simulation, layout-oriented yield modeling, defect-based approaches to fault modeling (including inductive fault analysis) as well as new design for manufacturability CAD strategies and defect/quality oriented testing methodologies.

Dr. Maly was elected an IEEE Fellow in 1990 and has been recipient or co-recipient of various awards including honors for his Ph.D. thesis, Ministry of Higher Education of Poland Research Award, Carnegie Mellon's Benjamin Richard Teare Teaching Award, AT&T Foundation Award for Excellence in Instructing of Engineering Students, Fellowship from Deutsche Forschungsgemeinschaft, SRC 1992 Technical Excellence Award, the Best Paper Award from the 1990 International Test Conference, the Best Paper Award from ESREF 94, the 1994 Best Paper Award from IEEE Transaction on Semiconductor Manufacturing, 1995 Best Paper Award from 1996 European Design, Test Conference, Eta Kappa Nu CMU Sigma Chapter Excellence in Teaching Award, the Best Paper Award from the 1997 International Test Conference and IEEE Circuits & Systems Society Golden Jubilee Medal.