

Evening Panel Discussion*

Tuesday, March 27

7:00pm-8:30pm

0.13 micron: Will the Speed Bumps Slow the Race to Market?



Organizer
Bill Alexander
Monterey Design Systems



Moderator
Jacques Benkoski
Monterey Design Systems

Description

Engineering departments face spiraling expectations to deliver more sophisticated products in less time while coping with the challenges of cutting-edge 0.13 micron technology.

Are the tools and methods ready and available to allow the shift to 0.13? Are designers prepared and armed to make 0.13 a mainstream production technology in an economical way within the next 24 months? In the past the next process technologies were brought up to volume production by shrinking existing circuit designs to the new technology. Will this approach work or is it necessary develop all circuits new for 0.13 micron?

In 0.13 micron technologies designers, CAD developers and manufacturers are faced with effects like following: Digital designs are beginning to behave like analog circuits. Physical phenomenon, which were not important before, need to be taken into consideration. Timing and noise are becoming intertwined. Design rules are more complex and don't shrink linearly. New optical effects for masks, yield issues, etc., etc. As the traditional methods are not working any more to shift existing designs to 0.13 micron technology the provocative question comes up; what are the "show stoppers" and what does it take to "let the show go on"?

A panel representing system and IC designer, EDA vendors, and semiconductor manufacturing executives will share their experiences, methods, and tools that they use or provide to tackle the 0.13 micron challenges and to accelerate design productivity.

Statements by Panelists:



Guy Dupenloup, Director Design Methodology, LSI Logic, Milpitas, CA

New 0.13 technologies enable the integration on a single silicon die of 20-30 million gates, hundreds of memories, high-speed I/O's, mixed-signal functions and embedded FPGAs.

The complexity of such chips dictates that a divide-and-conquer approach is used to enable concurrent design of blocks and support IP reuse. Chip planning and design data management are required to drive the implementation of blocks by multiple design teams, and guarantee that the chip is successfully assembled. All design activities that have remained based on a flat approach, in particular physical design and test, have to evolve towards a hierarchical approach.

* Reception starts at 6:30pm. Sponsored by Monterey Design Systems & Fujitsu Microelectronics

In addition to an increase in complexity, 0.13 processes come with an increase in signal integrity and silicon modeling difficulties. This includes voltage drops due to the resistivity of power rails, cross-coupling noise and cross-talk, inductance modeling, and on-chip temperature and process variation modeling. Techniques and tools are available or are being developed to address all those issues. However, the biggest challenge of 0.13 technologies certainly resides in assembling all components into a successful and efficient design flow. Design methodologies, customer engagement models supported by silicon vendors, and skills of design teams have to evolve substantially to both utilize the potential of 0.13 technologies and meet turn-around-time requirements that are dictated by time-to-market pressures.



Carlo Guardiani, Director of Statistical Design Practice, PDF Solutions, San Jose, CA

Multiple business and technological forces are vigorously shaking the ground in the proximity of the 0.13 μ m node region. The availability of integration capabilities in excess of 200K gates per sq. mm., cut-off frequencies in excess of several GHz, unprecedented current drive capabilities in the range of 1mA/ μ m, in conjunction with low resistivity Cu interconnects, low-K dielectric and novel CAD programs, such as physical synthesis and signal integrity tool, may make us think that the integration of entire complex systems in one single chip is no longer a far reach.

However, the equipment and R&D cost involved in the integration of 0.13 μ m technology capabilities are such that only very few silicon manufacturers will be able to afford them, and only very high volume or very high margin products will make sense in this scenario. At the same time, sky-rocketing costs of 192nm and 156nm litho, in conjunction with exponentially narrowing market windows, are fundamentally eliminating any margin for yield learning and product debugging cycles. Therefore, successful products in the 0.13 μ m era will be highly integrated mixed signal systems or MCMs, designed to achieve very high initial yield and extremely fast ramp to volume. In our opinion, the key ingredients to achieve this objective will be sound system design and prototyping capabilities, robust and innovative analog and M/S design methodology, perfect integration of design and manufacturing processes and thorough pre-silicon manufacturability analysis and optimization capabilities.



Christian Herdt, Project Manager Alpha Development Group, Compaq Computer Corp., Shrewsbury, MA

The Alpha microprocessor architecture will prolong its high performance lead in part through migration to more advanced technology. The three main obstacles to converting existing circuits to 0.13 μ m are: scaling power supply to accommodate the shrinking line widths leaves threshold voltages disproportionately large to maintain noise immunity; the large existing microprocessor design needs to be adjusted to significantly different transistors; the non-linear shrink threatens to leave performance and cost gains on the table.

The following solutions have been proposed to each of these hurdles. The Alpha microprocessor will use SOI (silicon on insulator) technology to maintain both noise immunity and high performance transistors, while benefiting from the lower diffusion capacitance. The resulting transistors break many dynamic, small signal and analog circuits on the chip; a complete redesign cannot be timely. An existing rule-based circuit analyzer has been adjusted for SOI technology and pinpoints the specific circuits that require design adjustments. To reach the full potential of the shrink, the specific design rules that scale non-linearly must be corrected. Such hand edits on a large full-custom microprocessor are insurmountable. In order to preserve the integrity of the database, a hierarchical compactor/corrector has been selected.



Charlie Huang, President CadMos Design Technology, San Jose, CA

The 0.13 micron silicon environment is very hostile. With this new technology comes a major increase in transistor count, shorter gate lengths, shrinking interconnect pitch, and higher clock frequencies, all contributing to increased electrical turbulence. Essentially, electrical problems arising from signal integrity such as long interconnect delays, noise and power supply variation need to be addressed in order to create working silicon.

As designers move to utilizing 0.13 micron technology, a number of major changes must be made to their existing design methodology, flow and tool suite. The responsibility for ensuring that a design will operate as expected in silicon can no longer be left as a back-end verification task performed by verification or product engineers. Design teams must manage signal integrity throughout all stages of the design process from early chip planning, library design, block implementation and chip assembly. In addition, design tools must be enhanced to accurately predict the important new effects arising from changes in 0.13 micron technology. Advances such as inductance effects in copper wires and floating body effects in SOI present significant new technical challenges. The tools must be also cognizant of the delicate tradeoffs involved between ensuring signal integrity while managing other important design metrics such as timing, power and area.



Atul Sharan, VP Marketing and Business Development, Numerical Technologies, San Jose, CA

As the semiconductor industry enters the 0.13 micron process generation, it faces a new challenge — the Subwavelength Challenge. At 0.13 micron, the feature sizes on silicon are substantially smaller than the wavelength of the 248-nm lithography equipment that is used to manufacture them. Although new generations of steppers continue to reduce laser wavelengths, silicon feature sizes are declining faster than lithography equipment advances.

In this subwavelength era, it is no longer safe for designers to assume that what they draw in GDSII will be exactly represented in silicon. The “WYSIWYG” (What You See Is What You Get) assumption that underlies the current EDA paradigm falls apart. In this presentation, we will discuss a set of technology solutions that span the design-to-silicon spectrum in and offer a transparent path to successful 0.13 micron design.



Ed Wan, VP Worldwide Field Engineering, UMC USA, Sunnyvale, CA

0.13 volume is anticipated to be as much as 30% of total volume of advanced foundries in 2003. Improvements in mask technology (strong phase shift) and process tooling are progressing accordingly. These developments continue to outpace the ability of design tools and methodologies to “keep up”, thereby widening the design gap. In particular, designers must be able to lay out even the most complex, multi-mega gate designs and then close timing. UMC has been taking measures to facilitate the transition to 0.13 and increase the probability of first-time success in 0.13 designs. These measures focus on the process integration of advanced materials, coupled with a comprehensive program of modeling, silicon verification, and product qualification of embedded memory

blocks.

- Calculations will show the necessity of novel materials (copper and SiLK low k dielectric) to maintaining Moore’s Law scaling from 0.18 to 0.13-micron.
- SiLK, with a k value of 2.65, offers a 25% reduction in wiring delay relative to FSG, providing a substantial advantage in design margin for timing closure. Thus, FSG is only recommended for 0.18 designs.
- Silicon verification, in concert with advanced modeling programs, is the heart of UMC efforts to ensure first pass design success. Ultra-accurate cell libraries based on an innovative VDSM characterization technology routinely achieve a 2% correlation with spice and measured logic delays.
- Due to extremely small SRAM bit cells sizes and large embedded SRAM memories up to 32Mbit, UMC memory development goes far beyond “silicon verification” to the point of product reliability qualification. Furthermore, embedded SRAM technology has built-in redundancy.
- WorldLogicSM is establishing a world standard for process technology. Our adoption of the IP standards of VSIA and our creation of a standard architecture for I/O, standard cells, and characterization methodology complement this.