

Plenary Speech 1P.3

The Expanding Use of Formal Techniques in Electronic Design

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Although Electronic Design Automation (EDA) tools allow some tolerance for features having only limited scope or not working in all cases, there is no tolerance for error in their final results. Since the beginning, EDA tools have included so-called “formal” techniques to ensure such error-free results. More and more, formal verification tools are being adopted as a necessary part of mainstream design flows to tackle the exploding verification challenge. In this keynote address, we will focus on some of these formal techniques; in particular, equivalence checking, property checking, and the combination of simulation with formal techniques — all of which play an important role in creating zero-defect results in state-of-the-art electronic design.

About Raul Camposano

Dr. Raul Camposano joined Synopsys in January 1994. He currently serves as Chief Technical Officer, being responsible for Research, IT and Advanced Technology. He previously served as General Manager of Synopsys’ Tool Business and in various Engineering positions. Prior to joining Synopsys, Dr. Camposano concurrently was the Design Technology Director for the German National Research Center for Computer Science and a Professor of Computer Science at the University of Paderborn, Germany. Between 1986 and 1991, Dr. Camposano led the project on high-level synthesis at the IBM T.J. Watson Research Center. Active in the EDA professional community, he also serves on various technical program committees and editorial boards worldwide and has published over 70 articles and three books on electronic design automation. He was elected Fellow of the IEEE in 1999. Dr. Camposano holds a B.S.E.E. from the University of Chile, and a Ph.D. in computer science from the University of Karlsruhe.