The next section of the tutorial begins with an overview of model order reduction techniques for analyzing large RLCK networks. Parasitic coupling impact on delay and noise will be discussed in detail. Analysis methods for electromigration on signal and power lines will be presented. Practical considerations in crosstalk delay, crosstalk noise and electromigration analysis of large ULSI designs will be presented.

Tutorial D3
3:30pm-5: 30pm

On-Chip inductance extraction and modeling

Duration: *2 hours, including Q&As*

Organizer: *Tak Young, Monterey Design*
Presenter 1: *David Blaauw, Motorola*
Presenter 2: *Rajendran Panda, Motorola*

With the VLSI feature sizes going deep submicron, interconnect issues have become dominant among the design issues. Interconnect issues now play a vital role in the performance of DSM circuits, and hence accurate analysis and careful design of interconnects are of critical importance in realizing quality designs with ambitious performance goals. Traditional models for interconnects considering only the R and C effects are proving to be inadequate in the DSM regime, especially for the global signal routes. The variation in delays and skews due to parasitic inductance is no longer ignorable; more so at GHz clock speeds. The "far coupling" effect of inductance is posing additional problems in analyzing and designing for possible signal integrity problems. Another trend affecting the performance and functional integrity of a design is the noise induced by the power supply network during abrupt power transience. Therefore, extracting and analyzing a detailed RLC model of the on-chip power interconnect, package, and decoupling structures is necessary to design a reliable supply network.

The first part of this tutorial will be devoted to provide the audience a comprehensive understanding of the various issues concerning inductance. We will then cover some of the popular approaches in modeling on-chip inductance, and analyzing the resulting large RLC networks, their complexity, and limitations. The objective here will be to equip a designer audience with an ability to evaluate and size up the claims of vendors for inductance extraction/analysis tools. The tutorial will then address various design issues and present methods to tackle noise in global signals and also noise induced by power supply network.

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