

## Tutorial Track D

Chair: Tak Young, Monterey Design

### Tutorial D1

**9:00am-12:00pm**

#### **Re-Connecting MOS Modeling and Circuit Design: New Methods for Design Quality**

*Duration: 3 hours, including a ½ hour break and Q&As*

*Organizer: Daniel Foty, Gilgamesh Associates*

*Presenter 1: Daniel Foty, Gilgamesh Associates*

*Presenter 2: David Binkley, UNC Charlotte*

Amid the blizzard of design-automation technologies, the analytical MOSFET models (and their associated model parameter sets) receive scant attention from the design community. However, these models and parameter sets are fundamental to the design process, since they represent the critical "communication link" between a design group and its wafer foundry. In particular, analog integrated circuit design is carried out at the transistor level; however, this fundamental aspect of analog design has not received much attention. The digital designer is also severely affected by slow MOS models, accuracy problems, and unpredictable model behavior.

The first part of this tutorial will examine the present "infrastructure" of MOS modeling for circuit simulation, with particular emphasis on how history has played a role at least as large as that of engineering. The tenor will be one of practical information for the circuit design "consumer" of transistor models. The second part of this tutorial will make the connection between MOS modeling and a modern approach to designing analog and digital integrated circuits. Here, it will be shown that a proper structural approach to MOS transistor modeling permits a more direct path to the key circuit information, allowing a designer to more carefully make decisions about critical design trade-offs.

### Tutorial D2

**1:00pm-3:00pm**

#### **Interconnect Modeling for Timing, Signal Integrity and Reliability**

*Duration: 2 hours, including Q&As*

*Organizer: Narain Arora, Simplex Solutions*

*Presenter 1: Narain Arora, Simplex Solutions*

*Presenter 2: NS Nagraj, Texas Instruments*

As VLSI technology shrinks to deep sub-micron geometries below 0.25um, the propagation delay due to interconnects (wiring) begins to dominate the total chip delay. In fact, parasitic delay due to interconnects are becoming limiting factors in determining circuit performance. An accurate estimation of the interconnects R (resistance), C (capacitance) and L (inductance) parasitic effects is thus essential in determining various interconnect related issues such as delay (timing), crosstalk, IR drop, power dissipation, electromigration, etc.

This course will cover interconnect issues in chip design, particularly its impact on timing and reliability of integrated circuits. Starting with defining interconnect as a parasitic element, we will cover interconnect scaling laws and discuss analytical and numerical methods of calculating interconnect R, C, and L. This will be followed by discussing techniques for extracting R, C and L at the chip level. We will also briefly cover verification and calibration of interconnect capacitance models using silicon test chip.