

Tutorial C2

1:00pm-3:00pm

Verification and Validation of Complex Digital Systems: An Industrial Perspective

Duration: 2 hours, including Q&As

Organizer: Li-C. Wang, UC-Santa Barbara

Presenter 1: Magdy S. Abadir, Motorola

Presenter 2: Li-C. Wang, UC-Santa Barbara

Verification and validation of complex digital designs (microprocessors, large ASIC, SOC, etc.) are very challenging in today's industry. Traditionally, they rely upon extensive simulation that typically consumes a large amount of compute and design resources. The effectiveness of traditional approaches becomes questionable as the size and complexity of industrial designs increase rapidly. This tutorial aims to provide an overview of practical verification/validation methodologies in use today. It will highlight the key challenges and how these methodologies are evolving. Designers, verification practitioners, as well as tool developers can all be benefited from learning the up-to-date technologies, and application issues/limitations of specific approaches.

We will first survey state-of-the-art techniques widely used in the industry, such as functional verification, directed and random testing, and equivalence checking. We will then describe advanced methods, including symbolic simulation, formal verification, ATPG-based verification, design error modeling, and design-for-debug/validation. During the tutorial, we will emphasize the relationship among validation, verification, and test. The tutorial will be primarily based on industrial experiences and real designs. Stories of success as well as failure will be presented. Strengths and weaknesses of various methodologies and a proper mix of tools in practice will be illustrated. Promising techniques and research directions for the future will be discussed.

Tutorial C3

3:30pm-5:30pm

Physical Verification at 0.13 Micron and Below

Duration: 2 hours, including Q&As

Organizer: John Ferguson, Mentor Graphic

Presenter 1: Andrew Moore, TSMC

Presenter 2: John Ferguson, Mentor Graphics

The advent of 0.13-micron and below production processes has increased capacity to multi-million gate designs. The data that must be managed is measured in hundreds of MB and billions of polygons. In addition, physical aspects of manufacturing must now be dealt with at the design stage, going far beyond traditional DRC.

The tutorial will present a survey of hierarchical verification and manufacturing issues that are required today and in the future. Example solutions of common problems in the field today will be shown, including CMP density and tiling, metal slotting, and antenna detection.