

Tutorial B3
3:30pm-5: 30pm

Issues in Deep Submicron State-of-the-Art ESD design

Duration: 2 hours, including Q&As

Organizer: Kaustav Banerjee, Stanford University
Presenter 1: Charvaka Duvvury, Texas Instruments

Oriented mainly toward the design and quality engineers, this tutorial will first outline the ever-increasing importance of ESD reliability for IC circuits, and then will review the effective design approaches for IC on-chip protection circuits. The effects of advanced process technologies and the impact on protection circuit design will be considered. The ESD protection strategy for the different I/O design applications, including high-speed RF applications will be addressed. In addition to low voltage CMOS, the tutorial will also consider SOI, BiCMOS, and High Voltage MOS. Finally, the recently developed simulation methods for ESD design optimization will be reviewed.

Tutorial Track C
Chair: Frank Lee, Avant!

Tutorial C1
9:00am-12:00pm

Application of Formal Verification to Design Creation and Implementation

Duration: 3 hours, including a ½ hour break and Q&As

Organizer: Noel Strader, Avant!
Presenter 1: Noel Strader, Avant!
Presenter 2: Gerard Memmi, Avant!
Presenter 3: Carl Pixley, Motorola

Successful design requires verification at both the design creation phase and the design implementation phase. We consider the design implementation phase to occur once a "golden" design description is available. Formal equivalence checks and their application to this phase are described. The design creation phase builds the golden design description from the design specification. Formal verification of this phase is less mature and more difficult. Best current technology in use is described here.

Formal equivalence checking compares RTL, gate, gate with clock trees, gate with scan, and gate with ECOs to the golden RTL. Also, the logical models of design primitives are formally compared with their transistor implementations, and those transistor-level views are compared with the final layout representations. The next big challenge in equivalence verification is to produce automatic tools to compare RTL to high-level models such as C, C++, SystemC or C-level.

Verification of the design creation phase is less mature. Here, several approaches are used including model checking (based on BDDs, SAT, or ATPG), symbolic simulation (STE) and theorem proving. There are many hybrid approaches proposed and used in semiconductor companies; finding still more effective approaches is a big challenge.