

## **Tutorial Track A**

Chair: Yervant Zorian, Logic Vision

### **Tutorial A1**

**9:00am-12:00pm**

#### **System-on-Chip: Embedded Test Strategies**

*Duration:* 3 hours, including a ½ hour break at 10:30 and Q&As.

*Organizer:* Dimitris Gizopoulos, University of Piraeus, Greece

*Presenter:* Yervant Zorian, Logic Vision

Spurred by technology leading to the availability of millions of gates per chip, system-level integration is evolving as a new paradigm, allowing entire systems to be built on a single chip. This tutorial presents the state-of-the-art in system-level integration and addresses the strategies and current industrial practices in the test of system-on-chip. It discusses the requirements for test reuse in hierarchical design, such as embedded test strategies for individual cores, test access mechanisms, test interface standardization, optimizing test resource partitioning, and embedded test management and integration at the System-on-Chip level.

### **Tutorial A2**

**1:00-3:00pm**

#### **Design and Test of Low Voltage CMOS Circuits**

*Duration:* 2 hours, including Q&As

*Organizer:* Kaushik Roy, Purdue University

*Presenter 1:* Kaushik Roy, Purdue University

*Presenter 2:* Ali Keshavarzi, Intel Corp

This tutorial focuses on challenges of low voltage CMOS design and test. As technology scales leakage and leakage control becomes critical for design and test of integrated circuits. We explain testing techniques for intrinsically leaky ICs. This tutorial covers the following topics: Scaling of MOS devices; Low-voltage low-power CMOS design style; Cross-talk issues and predictable design, Transistor threshold scaling for high performance designs; Leakage current in CMOS circuits, Leakage control techniques such as multiple VT CMOS, dynamic VT CMOS, transistor stacking; Testing of low voltage low threshold CMOS circuits under elevated background leakage.