

Adaptive IDDQ: How to set an IDDQ Limit for any Device Under Test

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Abstract

The combination of deep sub-micron technologies together with System on Chip complexity has brought the Device Under Test (DUT) Quiescent Supply Current (IDDQ) into the Milliamps (mA) range. This IDDQ level, modulated by Electrical Parameters and Critical Dimensions Process spreads, makes almost impossible to detect the small current increase caused by the presence of a defect into the DUT.

The integration of a limited size IDDQ cell into the DUT, combined with Automatic Test Equipment (ATE) measurements and calculations allows to define an IDDQ limit for every DUT during Electrical Wafer Sort (EWS) revitalizing a powerful way to prevent defective chips can reach the application field.

In the today mass production CMOS technologies (.18micron and .13micron) is quite common to deal with high levels of Quiescent Supply Current, making very critical and unsafe the IDDQ testing.

If $IDDQ_g$ is defined as the "Quiescent Current associated to a Good DUT" and $IDDQ_t$ as the "Quiescent Current Threshold" to be used as limit by the ATE, in the relationship:

$$IDDQ_d = IDDQ_g + I_{sc} > IDDQ_t \quad (1)$$

the smaller the level of I_{sc} (extra current due a single defect into the chip) the highest the efficiency to capture and reject Defective devices. Unfortunately $IDDQ_g$ is heavily affected by Process Variations and during mass production $IDDQ_g$ can easily move one order of magnitude, (500uA to 5mA) while I_{sc} stays in the range of few hundreds of micro-Amps. The use of differential IDDQ test method can only mitigate the described problem.

A more accurate value for $IDDQ_t$ can be set deriving it directly for every DUT. The basic simple IDDQ cell, embedding two arrays of N and P Mos (fig1 and fig.2), is integrated into the chip and made reachable by EWS needle probes thanks to the addition of only two pads.

The linkage between the (normalized) I_{sub} (sub-threshold current) and the total number of N and P Mos devices (with their channel widths W) in Off conduction state: $\sum W_{Noff}$, $\sum W_{Poff}$ (during the IDDQ test at V_{dd1} voltage supply) is expressed by

$$IDDQ_g(V_{dd1}) = I_{subN}(V_{dd1}) \sum W_{Noff} + I_{subP}(V_{dd1}) \sum W_{Poff} \quad (2)$$

To solve the (2), finding the unknown : $\sum W_{Noff}$, $\sum W_{Poff}$ (which will become proprietary number of the DUT in the specific IDDQ test file) at least one Good sample has to be identified and its I_{subN} and I_{subP} measured on its IDDQ cell in the most accurate possible way (ATE to use Precision Measurement Unit or Dedicated High Resolution Hardware) . Doing that at two different DUT Supply voltages will provide the I_{sub} and $IDDQ_g$ constants to solve the system of equations based on (2). The now defined $\sum W_{Noff}$, $\sum W_{Poff}$ stored into ATE memory will be applied, during EWS, in combination with I_{subN} , I_{subP} measured for every DUT. During EWS the ATE will compute $IDDQ_g$ as DUT is a Good device. The $IDDQ_t$ limit will therefore be set having reduced the huge $IDDQ_g$ noise caused by Process Parameters Variations.

$$IDDQ_t = IDDQ_g + I_{sc} < IDDQ_d \quad (3)$$

Into (3) the I_{sc} will be close to 170uA for a (typical) .18micron technology to 250uA in a .13 one (@25°C).

The IDDQ cell inserted into the Digital Libraries of every new CMOS technology, is integrated into chip layout with negligible impact on die area and pads count.

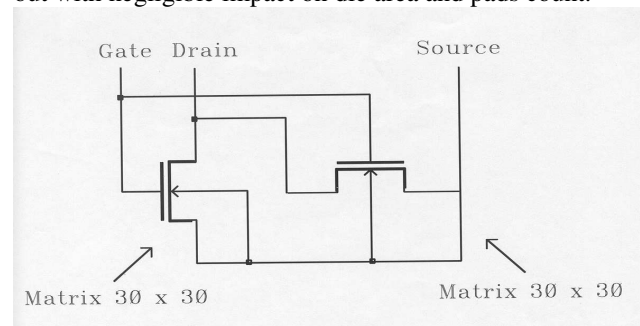


Fig 1: Gate, Source and Substrate connected at DUT Ground, Drain connected at Pad 1

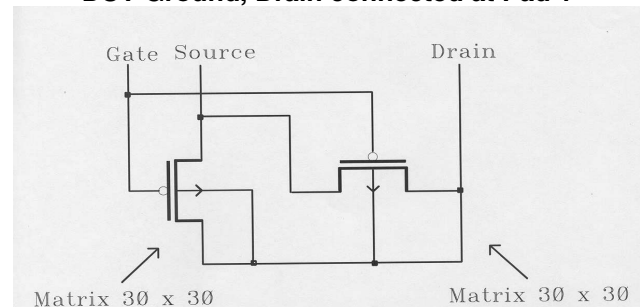


Fig 2: Gate, Source and Substrate connected at Pad 2, Drain connected at DUT Ground