Fault tolerant ICs by area-optimized error correcting codes

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Abstract

Integrated Circuits suffer from malfunctioning because of permanent production errors, and transient or permanent errors during operation. ICs can be made tolerant for these errors by building in self-repair using (known) error correction codes. These are now optimized for minimum silicon area, which essentially differs from using the classical criterion of minimal code redundancy. As compared to majority voting, our area-optimized Hamming codes and product codes offer sufficient fault protection for less than half the silicon area overhead.

ICs suffer from two types of errors, namely hard (permanent) such as opens, shorts and stuck-ats, and soft (transient), for instance due to alpha particles, *EMC*, noise and timing glitches. They can be protected by fault tolerant design [1].

We consider the protection of Boolean circuits by error correction codes [2, 3, 4]. Berger and Bose-Lin codes were proposed earlier for error *detection* [5]. We propose the use of *area optimized* Hamming and product codes for *correction*. Our design criterion is: minimize additional circuit area.

The method we propose in order to protect design C is shown in the figure. Circuit E, the encoder, is added, augmenting the output signals of C, to obtain code words with the required minimum Hamming distance for correction. Decoder D performs the detection and correction. Both E and C are protected from errors.

A known method of fault tolerant design is majority voting [6]. If there is no defect, the three outputs are equal, while an error in one of the outputs can be corrected by majority voting. The cost is dominated by the encoder (2 copies of C). The decoder and corrector have a fixed overhead per output line.

For the least-area Hamming code, the encoder generates parity bits. The fast *Ortolog* tool [7] is used for logic synthesis of E to search for the smallest area Hamming code, which depends on the original circuit complexity and number of inputs. The decoder and corrector sizes depend on the number of outputs.

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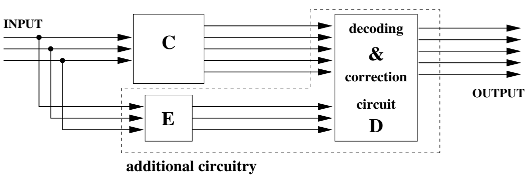

Area μm^2	orig.	Maj.v.	Ham.	product
design	88605	88605	88605	88605
encoder		177210	43911	82512
decoder		882	3510	1800
corrector		implied	756	756
factor	1.0	3.01	1.54	1.96
unprot.	100%	1.0%	4.5%	1.4%

For the optimized product code, all output bits are arranged in a 2-dimensional matrix and extended with a parity for each row and column. The decoder consists of trees of $EXOR$ gates with AND gates to combine row and column parities. Area optimization of the encoder is done by re-ordering the outputs in the matrix.

The table shows the three methods applied to a design with 14 inputs and 14 outputs, specified as a PLA of 175 cubes. The area overhead factors range from 1.5 to 2, versus 3 for majority voting. The remaining unprotected area, as percentage of the original circuit, measures the level of protection. While majority voting and product methods yield a good protection, the Hamming method leaves a larger region unprotected (4.5% of the original area).

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