

TRACS - TRansient Activity Checking with Scan Cells

Jose Miguel Vieira dos Santos

ISEP - Instituto Superior Engenharia do Porto - Portugal

jmvs@dee.isep.ipp.pt

Keywords: *On-line testing, Temporary faults, DFT, BST, Dependable VLSI circuits.*

Introduction

Inside digital systems, errors are a result of *temporary* and *permanent* faults, these last requiring less redundancy usually to be detected. Beyond traditional techniques as duplex with comparison or Self-Checking designs, one recently presented, and relevant in this context, is named Concurrent Scan Test (CST) [1].

CST enhances the IEEE 1149.1 (BST) infrastructure to detect faults concurrently, adding to every relevant scan cell the ability to compare node signals to the content of its internal flip-flop and synchronizing itself to the mission circuit upon a match.

Temporary faults are mostly caused by power supply and electromagnetic noise, radiation (a growing concern as geometry shrinks) and physical degradation [2], a first step for permanent faults as I_{DDQ} and Thermal monitoring supporters claim. Pointed as responsible for 90-99% of the errors, they are detectable with traditional techniques but the overhead impacts the reliability, mainly in a single VLSI chip. However, the hardware being not injured by these faults, many applications allow to reduce physical redundancy, a feature essential in new ICs.

The TRACS principle of operation

TRACS is a low cost technique reusing the IEEE 1149.1 std infrastructure to detect unexpected node activity. Designed for a *critical-but-not-life-critical* system specified to work in a noisy environment [3], TRACS enhances CST handicap to deal with the low probability of detecting temporary faults, and targets the faults behaving asynchronously and leading to node activity without the required stimulus.

TRACS was tested with a 5600 gates mission circuit, including 17 latches, and a boundary scan chain with 37 cells (17 PI + 20 PO). As shown in the figure, the *Primary Inputs (PI)* cells generate the Input Detect (I_D) signal, while the *Primary Outputs (PO)* cells provide the Transition Detect (T_D) signal, both feeding the Error indication logic. Following each input changing, the cells capture and hold the node data, as a normal latch does, to be compared to node activity. If any of these nodes changes state, by unexpected reasons, an error is signaled.

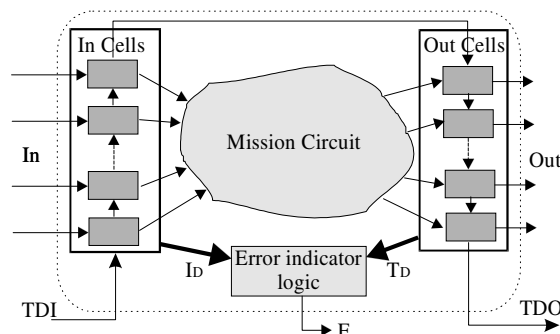


Fig.1- TRACS principle of operation

The programmed FPGA has $F_{max}=27$ MHz and faults were injected simulating S@ and S-open types (ideal and resistive degradation for both) and cross-talk. The results below show a correlation between the probability of detecting unexpected activity and the interval without forced activity, except for the S-open type.

Table 1- Percentage of faults detected

Fault type	Faults detected (%)		
	Frequency / Fmax		
	0.8	0.5	0.2
S-@ (0-1)	47	56	57
S-@ (R variable)	86	91	94
S-open	12	8	7
S-open (R variable)	68	71	73
Cross-talk	76	78	78

A major feature is the low cost, as hardware overhead to the 1149.1 std infrastructure is about 5% (say less than 1% to the mission circuit) and works without external support. Since TRACS needs no test patterns, observation points can be randomly scattered but, using relative references only, it is unable to detect permanent faults.

Presentation partially supported by Fundação para Ciência e Tecnologia.

Selected Papers

- 1 - J. M. V. Santos, "Concurrent Scan Monitoring and Multi-Pattern Search", *Proceedings of the 6th IEEE Int. On-Line Testing Workshop*, pp.107-111, Spain, July 2000.
- 2 - M. Renovell, F. Azais, Y. Bertrand, "Analysing Relationship between Defect and Fault Model", *Compendium of Papers, IEEE European Test Workshop*, pp. 151-155, 1998.
- 3 - J.M.V. Santos, "TRACS-Sistema Tolerante a Falhas em Ambientes Industriais", *Int.Rep., MERCI Grp*, October 2000.