

Power Constrained Test Scheduling with Low Power Weighted Random Testing

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I. INTRODUCTION AND TECHNICAL OBJECTIVES

In the past, the problem of power dissipation during test was only a minor issue since the test was performed at a speed lower than the normal operation speed. Conversely, today's circuits are tested at higher clock rates, if possible at the circuit's normal clock rate (at-speed testing). Second, the switching activity of the circuit during self-test is significantly larger than during normal operation. Therefore, the power dissipation during test can be much larger than during normal operations. Circuits have been reported to be burn during test. Therefore, reducing power dissipation during test application becomes an important objective in BIST design.

Energy consumption is another critical concern in design and test of portable computing and wireless communication systems. The market acceptance of mobile applications and notebook computers heavily depends on the operation time per battery pack. To enhance battery life, it is very important to reduce energy consumptions during on-line testing. Energy conscious BIST can be used efficiently in on-line testing for battery operated applications.

CMOS technologies have very low power/energy consumption when signals are not switching. The majority of the energy dissipation in the current day's technology is due to charging and discharging of load capacitance of logic gates, which occurs when logic gates undergo signal transitions. Hence, in order to reduce power/energy consumptions in BIST, it is desirable to reduce the switched capacitance during the test mode.

Random pattern testing is widely used in BIST because it does not require large memory overhead while achieving high fault coverage with a limited number of input vectors. Energy consumption during random test is proportional to the product of the test time (test length) and the average dynamic power. There are three main objectives in BIST design:

- to minimize test length (test time)
- to minimize power/energy
- to maximize fault coverage

To achieve the BIST objectives, several different test techniques have been proposed. The conventional weighted random pattern testing technique (WRP) reduces the test length by optimizing signal probabilities (probability that a signal is logic ONE) or weights of the inputs, but it does not consider any reduction of average power. On the other hand, DS-LFSR [3] reduces the average power by operating one of the two linear feedback shift registers at slow speed. However, it does not reduce the test length. In order to reduce both the test length and average power, Zhang and Roy proposed a low power BIST (LPBIST) [2] technique, in which both signal probabilities (probability of signal being logic ONE) and activities (probability of signal switching) at the primary inputs are optimized, hence both the average power and the test length are reduced significantly. For ISCAS benchmark circuits, while the average of power reduction by using DS-LFSR is 19%, the average of power reduction by using LPBIST technique is as high as 73%.

Proper scheduling of test during BIST can also reduce power consumption. The power constraints of a system are defined for normal operation, during which only a small number of logic blocks are active, while others are idle. During test, if we apply test patterns to all the blocks simultaneously the power constraints can be easily violated. In order to avoid unwanted failures during test, Chou and Saluja [1] proposed a constrained optimization algorithm for test scheduling, in which the overall test length is minimized with the constraint of power limit. They assumed that both test length, fault coverage and power are invariant with respect to the scheduling of test. For systems in which different circuit blocks have common primary inputs, the above algorithm cannot be applied, because different blocks with common primary inputs may have conflicting testability requirements, and the test length or fault coverage can vary if different circuits are tested simultaneously or independently. Furthermore, although energy con-

sumption and power dissipation are very crucial issues for portable applications, the above algorithm does not consider any strategies to reduce the energy/power during test.

In this paper, we propose a novel test scheduling approach which incorporates the LPBIST technique. For each circuit block, the power dissipation is minimized and the fault coverage is maximized by optimizing the primary input signal probabilities and activities. Although the test length for each circuit block is fixed, the overall test length is minimized by carefully scheduling test under the constraint of average power. In our approach, the fault coverage and average power for a block are no longer fixed numbers, and they may vary with different test schedules. Let us consider a circuit block A in a large system. If block A is tested as a separate block, then the optimization of signal probabilities and activities at inputs of A will not affect other blocks. Conversely, if the block A is tested parallelly with other blocks, then we can view all the scheduled blocks (including A) as one hierarchical circuit block, and the optimization of signals at the inputs of A will be affected by other blocks in the hierarchy. The signal probabilities at the primary inputs of the hierarchical block are optimized such that the fault coverage in the block is maximum, while the primary input signal activities are optimized such that the total average power in the hierarchy block is minimum. The optimal input probabilities and activities can be different depending on whether A is tested parallelly with other blocks or tested alone. Hence both the fault coverage and average power in block A depends on how the test is scheduled. In summary, proper test scheduling maximizes the fault coverage by optimizing the primary input signal probabilities, minimizes the average power by optimizing the primary input signal activities, and reduces the overall test time because more blocks can be tested simultaneously at any given time instant.

II. RESULTS

We used the nine ISCAS benchmark circuits to construct a random circuit. We randomly chose inputs from different benchmark circuits and tied them together to form common primary inputs. We used our algorithm to schedule test and used a fault simulator to obtain the actual fault coverage. All the benchmark circuits were technology mapped to circuits consisting of only AND, NAND, OR, NOR, INVERTER and BUFFER. Our technique reduced the test length from by 66%, reduced energy by 50% units while achieving fault coverage similar to WRP.

III. CONCLUSIONS

In order to keep power dissipation within some pre-defined range, a careful test scheduling is necessary for very large systems. In this paper, we propose a test scheduling algorithm which incorporates the LPBIST technique. Signal probabilities at the PI's are optimized for fault coverage, while activities are optimized for average power dissipation. Since LPBIST significantly reduces the average power dissipation of every circuit block, our technique not only achieves fault coverage similar to WRP, but also considerably reduces the energy and test time.

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