

## An approach for designing on-line testable state machines

P. K. Lala  
Department of Computer Science  
and Computer Engineering  
University of Arkansas  
Fayetteville, AR 72701

M. G. Karpovsky  
Department of Electrical and Computer  
Engineering  
Boston University  
Boston, MA 02215

This paper proposes a new approach for designing state machines that have built-in capability for enhancing on-line and off-line testability. The architecture of the proposed state machine is shown in Fig.1. The next state logic is designed using transmission gates and tri-state buffers only. The outputs of the next state logic are transferred into Q by using the preset and the reset inputs associated with each bit of Q, instead of using the system clock. In other words, Reg. Q operates in asynchronous mode. The number of buffers required is equal to the number of states in a machine, and the number of transmission gates is equal to the number of specified next states. The on-line testing capability is achieved by EX-ORing the outputs of the two registers in a machine, and checking for even parity at the outputs of the EX-OR gates. The number of EX-OR gates equals the length of the registers, plus those needed for parity checking.

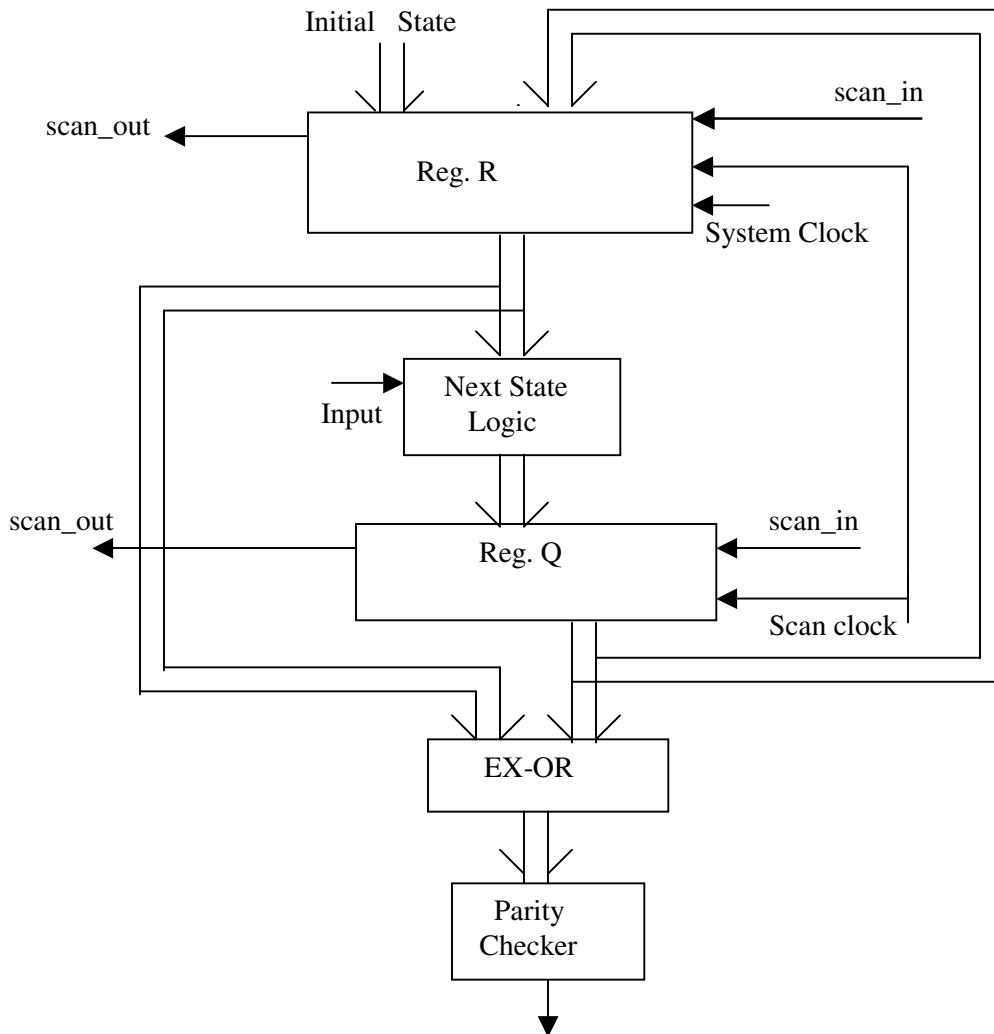


Fig. 1 Proposed architecture of state machines