

Analysis of Bit Transition Count for EDAC Encoded FSM

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Abstract

The focus of this paper is to present a bit transition count analysis for various Error Detection And Correction (EDAC) schemes through a detailed simulation. The simulation also brings out the impact of various EDAC schemes - linear, BCH, m-out-of-n, Berger and SEC-MUED - on bit transition count with respect to number of FSM partitions under different partitioning objective functions for low power. A decrease up to 30 percent in bit transitions count under the three partitioning objectives has been observed.

1. Analysis of Bit Transition Count in EDAC Encoded FSM

Here we present a detailed power analysis for fault tolerant FSMs based on error detection and/or correction codes namely linear codes, cyclic linear (BCH), Berger, m-out-of-n and SEC-MUED codes [1,2].

The bit transition count for Un-partitioned FSM (UFSM) encoded for different error correcting code (ECC) and uni-directional (UD) cases are shown in Figs. 1 and 2. The analysis shown includes randomly generated

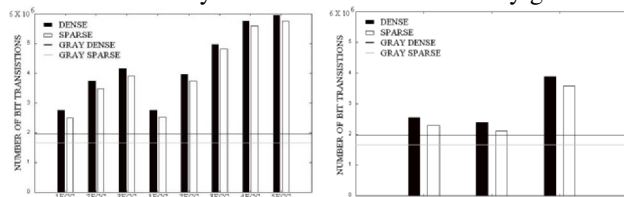


Figure 1. Symmetric

dense as well as sparse STG. The horizontal lines in the graph gives the Bit Transition Count (BTC) for normal state assignment, which has minimum hamming distance of one.

The bit transition graphs shown in Figs. 1 for symmetric and 2 for Uni-directional have a sharp increase in bit transition count for the encoded cases over the normal state assignments. By resorting to partitioning of the FSM and assigning suitable encoding schemes one can considerably reduce the sharp increase in bit

Figure 2. UD

transition count.

Three different OBF are chosen for partitioning the EDAC encoded FSM: **a)** Partitions having equal number of states. **b)** Minimum number of edges across partitions. **c)** Partitioning based on the edge weights (the edge weight is the relative number of transitions across nodes) being acquired by prior simulation run of the FSM.

The percentage decrease from their un-partitioned case is depicted as graphs in Figs. 3, 4, 5(for symmetric) and 6(UD). It is inferred from these graphs, in general, as the number of partitions increases irrespective of the partitioning objectives and the encoding schemes, the bit transition decreases.

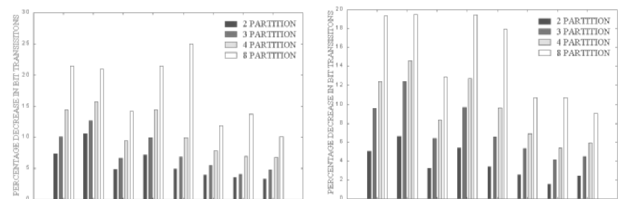


Figure 3. OBF-1

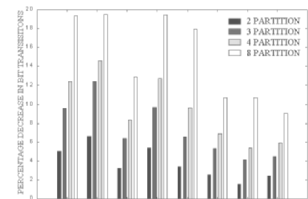


Figure 4. OBF-2

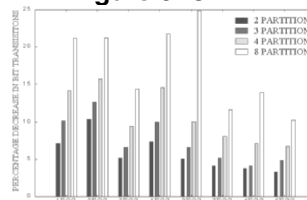


Figure 5. OBF-3

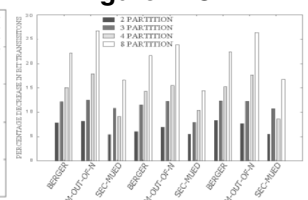


Figure 6. 3-OBFs for UD

2. Conclusion

This paper presents a detailed analysis of the bit transition count for the different EDAC encoded schemes, for un-partitioned and partitioned cases. The simulation results were obtained using the WARF FSM Power Analyzer (WARFFPA) tool.

3. References

- [1] D.G. Hoffman et.al, "Coding Theory The Essentials", 1991 Marcel Dekker, Inc.
- [2] D.K.Pradhan, "Fault tolerant computing", Prentice Hall, Eaglewood Cliffs, New Jersey 1996.