

Radiation test methodology for SRAM-based FPGAs by using THESIC+*

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Abstract

The paper presents a radiation test methodology for Xilinx Virtex FPGAs based on the THESIC+ system.

1. Introduction

Benefits resulting from the adoption of SRAM-based FPGAs as design target technology in space applications are manifold: increased gate density and speed/performance, low power, no NRE (Non Refundable Engineering) costs, and a practically unlimited reconfiguration ability. These devices, however, exhibit a potentially high susceptibility to Single Event Upsets (SEU), due to the presence of a large number of configuration memory cells. As fault injection alone is not able to reach every circuitry inside an FPGA, radiation ground testing is mandatory in order to perform the analysis on a larger set of SEU upsets. In order to perform a radiation ground testing, a flexible test apparatus and a proper methodology are required. They are to allow an easy evaluation of the features contributing to the upset rates of the FPGA device, including both the configuration and the readback management circuits, this aiming at investigating the possibility to implement highly re-configurable systems for space applications. The methodology proposed makes use of THESIC+, a system devoted to hardware/software set-up of Single Event Effect test experiments [1].

2. Test methodology

A proper customization of THESIC+ has been accomplished in order to perform the test on Xilinx Virtex FPGAs and, in particular, ad hoc daughter board has been developed for XQV300 devices. The specific test vehicle architecture adopted is the TOSHIRO (Tolerance by SHifted and ROtate operands) fault tolerant scheme [2]. TOSHIRO is a Triple Modular Redundant (TMR) ALU able to tolerate Common Mode Failures (CMF). CMFs are a particular class of failure that impairs the tolerance ability

of redundant systems and, as pointed out in [3], may occur in SRAM-based FPGAs due to a single source of radiation. The TOSHIRO scheme was extensively evaluated by means of fault injection and was proved able to tolerate 100% of CMF affecting the device's internal programmable blocks.

The application that has been developed for the XQVR300, from now on DUT (Device Under Test), is aimed at evaluating both the possibly increased fault tolerance ability of the TOSHIRO scheme, with respect to a traditional TMR scheme, and the configuration failure rate for the DUT that undergoes very frequent re-configurations. In the first case, whenever a mismatch is found between TOSHIRO (or TMR) output and the expected value, the ion beam is switched off, the bitstream is on-line compared with the original one and the number and position of altered bits are store into the THESIC+ memory. After that, the TOSHIRO (or TMR) configuration is refreshed and the experiment restarted. To evaluate the effects on the device configuration, we configure the DUT alternatively with the TOSHIRO scheme and the classical TMR. The configuration success is evaluated every time a bitstream is applied.

The experiment, scheduled for the end of May 2003, will be conducted at Cyclone facility at Louvain-la-Neuve, Belgium, using heavy ions covering a wide range of LET (Linear Energy Transfer).

References

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