

Fault Injection in Digital Logic Circuits at the VHDL Level

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Abstract

This paper presents hardware-based techniques for transient and permanent fault injection in VHDL descriptions of both combinational and sequential digital circuits. The designer can choose the fault injection rate, which may vary from 100% (permanent fault) down to .01% (transient fault).

1. Introduction

The first step in a modern digital system design is to specify it in a high level language such as VHDL. Before and after the translation of a description into an actual implementation, the design needs to be evaluated based on several criteria, e.g. testability, power consumption, etc. The capacity to ascertain the testability of a system written in a modeling language such as VHDL allows design modifications to achieve the desired goal. The proposed fault injection system, a specially designed block of VHDL, will be contained within the instruction VHDL of a system.

2. Fault Injection in VHDL

The proposed fault injection system shown in Figure 1 is comprised of five blocks with three levels of hierarchy. To invoke the system one component instantiation block is necessary for each data word where faults are to be inserted.

A key component of the fault injection system is the ability to insert transient faults at desired intervals. To accomplish this task the injection system uses pseudo-random sequences. Pseudo-random sequences of maximal length are generated using LFSR's. The two 16-bit LFSR's run in parallel constantly generating pseudo-random sequences. Based on the percentage of time that is chosen to insert a fault, a certain number of bits in the two LFSR's are compared by the fault injection logic

block. If that number of bits matches, then a fault is inserted into the system.

The Fault Injection Logic block is the heart of the injection system that incorporates data from the two LFSR's and also from the One-Hot Encoded shift register. The block monitors the control inputs to the circuit to evaluate whether it needs to perform transient or permanent fault injection in the data that is sent to it.

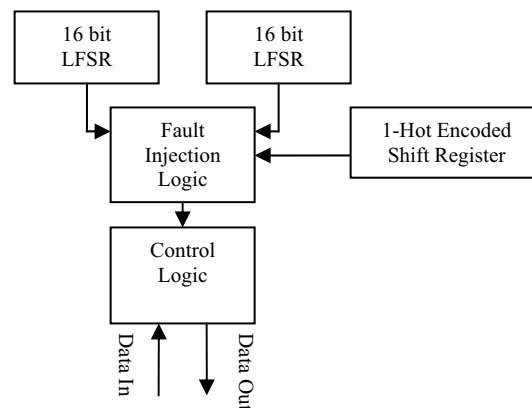


Figure 1. Fault Injection System.

The Control logic allows the user to change rates of fault insertion during operation by means of a 4-bit control code, operating in parallel 16 different Fault Injection Logic blocks. If the system is active, then a fault is inserted on the data word coming into the system and directed to the data out word.

3. Conclusion

The proposed injection technique offers a designer the use of a VHDL package to insert a fault on any signal within the block of a VHDL code. It allows the injection of transient faults randomly across a data word, and allows the insertion of a permanent fault at any point.